

PROJECT NAME : CAL51/CLA61/CAL71
PCB NO :

Dell / Compal Confidential

Schematic Document

AMD Raven

AMD R17M-M2-50 (23 X 23mm) +GDDR5 x4

2017-11-09 Rev: 1.00 (A00)

@ : Un-pop Component

R5_PC@/R7_PC@/R3_PC/R5_PR@/R7_PR@/R5_PR_R3@/R7_PR_R3@:APU PN

45@: HDMI LOGO

PCB@/: MB part number

4G_S@/4G_M@/4G_H@/2G_H@/2G_M@/2G_S:

VRAM Strap Pin:

Vram 2G:S2G_R3@ / H2G_R3@ /M2G_R3@

Vram 4G:S4G_R3@ / H4G_R3@ /M4G_R3@

DIS@: GPU only

M50_R3@:GPU R3 PN

UMA@/:UMA only

TI@/PARADE@/NRDSA@ : SATA

3234@ :Audio

EMI@/ESD@/RF@ : EMI, ESD ,RF Component

@EMI@/@ESD@/@RF@ : EMI, ESD,RF unpop

KBBL@:for KB backlight use

PTP@/NPTP@/TP_WAKE@:Touch pad

TYPEC@/NOTYPEC@:TYPEC

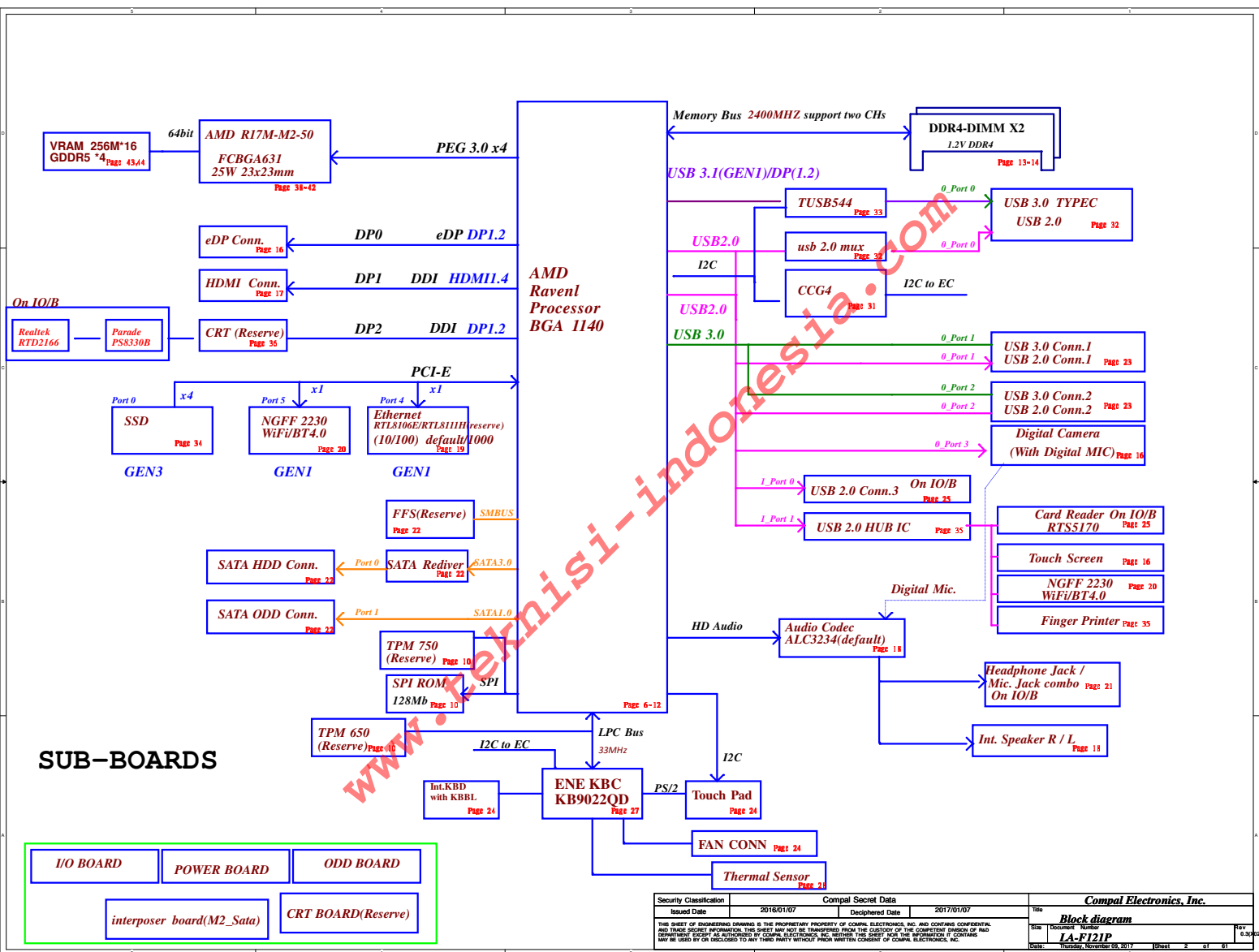
Typec@EMI@/Typec@ESD@: EMI/ESD typec component

CRT@:D-sub TPM@:TPM FFS@:free fall sensor

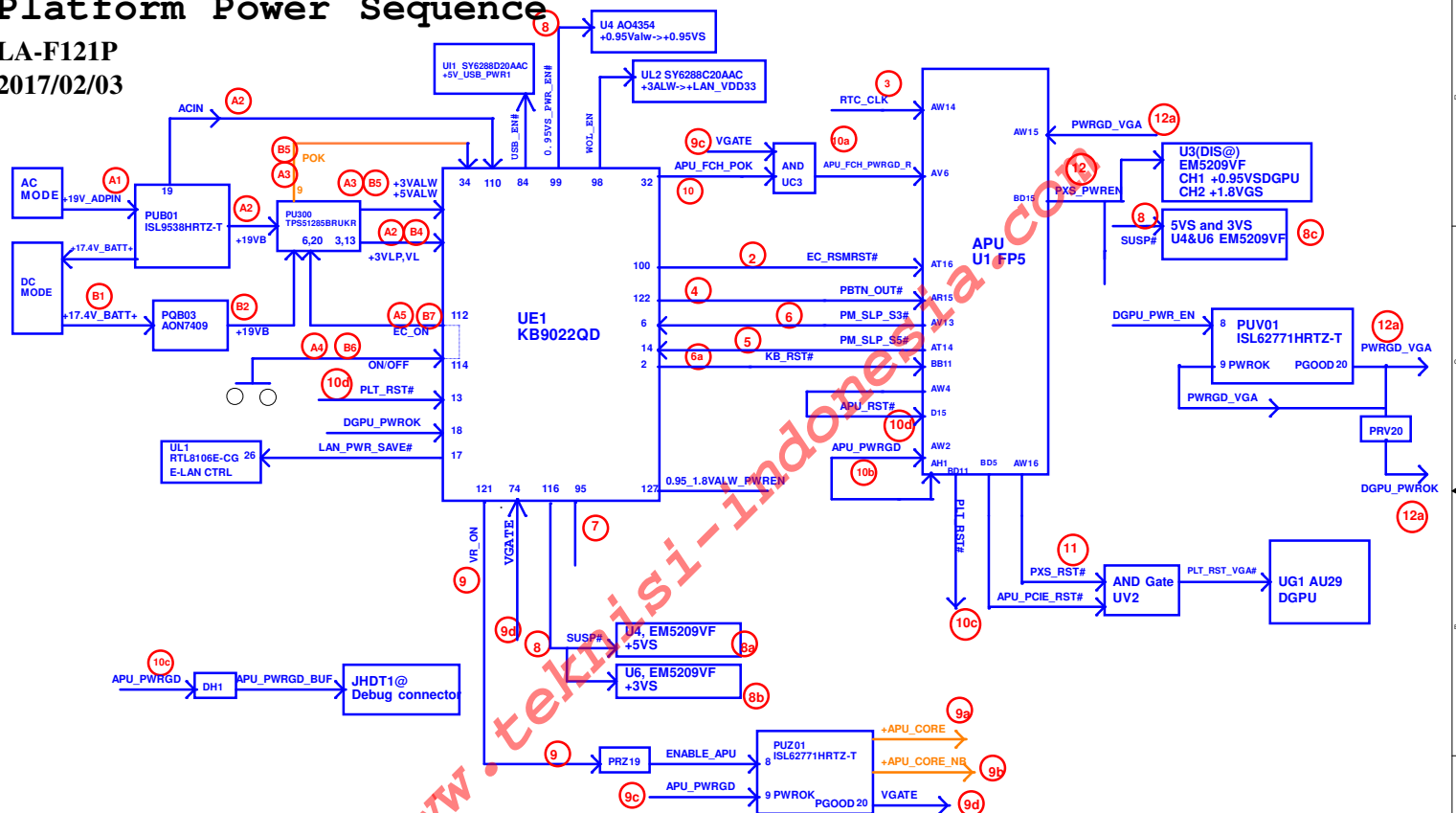
HDT@ /Debug use

MODS@:moderd standby

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2017/02/03



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC_AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	Raven EVT UMA
1	Raven EVT DIS
2	Raven DVT1 UMA
3	Raven DVT1 DIS
4	Raven DVT2 UMA
5	Raven DVT2 DIS
6	Raven Pilot UMA
7	Raven Pilot DIS
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

SMBUS Control Table

	SOURCE	BATT	Charger	DIMM	Thermal Sensor	FFS	CRT
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V				
EC_SMB_CK2 EC_SMB_DA2	KB9022Q				V		
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q						
APU_SCLK0 APU_SDAT0	APU			V		V	V
APU_SCLK1 APU_SDAT1	APU						
APU_SIC APU_SID	APU				V		


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PCI EXPRESS(GFX)

Lane 1	PEG (AMD)M2-50
Lane 2	PEG (AMD)M2-50
Lane 3	PEG (AMD)M2-50
Lane 4	PEG (AMD)M2-50
Lane 5	RV2 NA
Lane 6	RV2 NA
Lane 7	RV2 NA
Lane 8	RV2 NA

USB3.0	
0_Port0	TYPE C
0_Port1	USB3 connector 1
0_Port2	USB3 connector 2
0_Port3	progaming DP signal
1_Port0	
1_Port1	
USB2.0	
0_Port0	TYPE C
0_Port1	USB connector 1
0_Port2	USB connector 2
0_Port3	Camera
1_Port0	USB connector 1(D/B)
1_Port1	USB HUB
PCI EXPRESS(GPP)	
Lane 1	NVME SSD
Lane 2	NVME SSD
Lane 3	NVME SSD
Lane 4	NVME SSD
Lane 5	10/100 LAN(GIGA RESERVE)
Lane 6	NGFF Card (WLAN)
Lane 7	use sata interface
Lane 8	use sata interface
SATA	
SATA0	HDD
SATA1	ODD

Symbol Note :

 : means Digital Ground

 : means Analog Ground

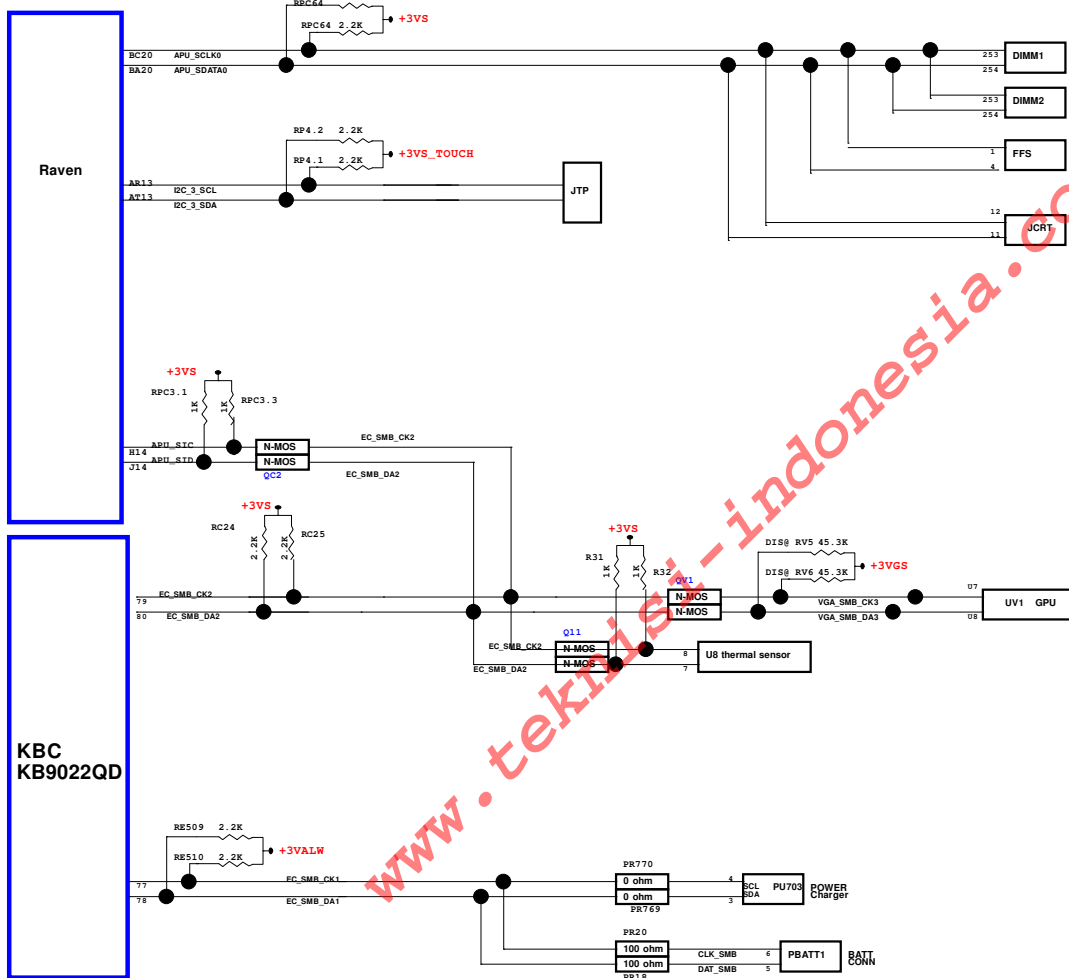
Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+SDC_IN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+APU_VDDCORE	Core voltage for APU	ON	OFF	OFF
+APU_VDDSOC	VDDSOC voltage for APU	ON	OFF	OFF
+3VALW_APU	3V, always for APU	ON	ON	ON*
+0.8VALW_APU	0.8V, always for APU	ON	ON	ON*
+1.8V_ALW_APU	1.8V, always for APU	ON	ON	ON*
+0.8VS	0.8V sustain for APU	ON	OFF	OFF
+VGA_CORE	VGA core power rail for GPU	ON	OFF	OFF
+1.35V_MEM_GFX	+1.35VS power rail for GPU and VRAM	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	0.95V power rail for GPU	ON	OFF	OFF
+3.3V_VDD_PIC	3.3V power rail for PD chip	ON	OFF	ON*
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VS	System +3VS power rail	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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SMBus Block Diagram



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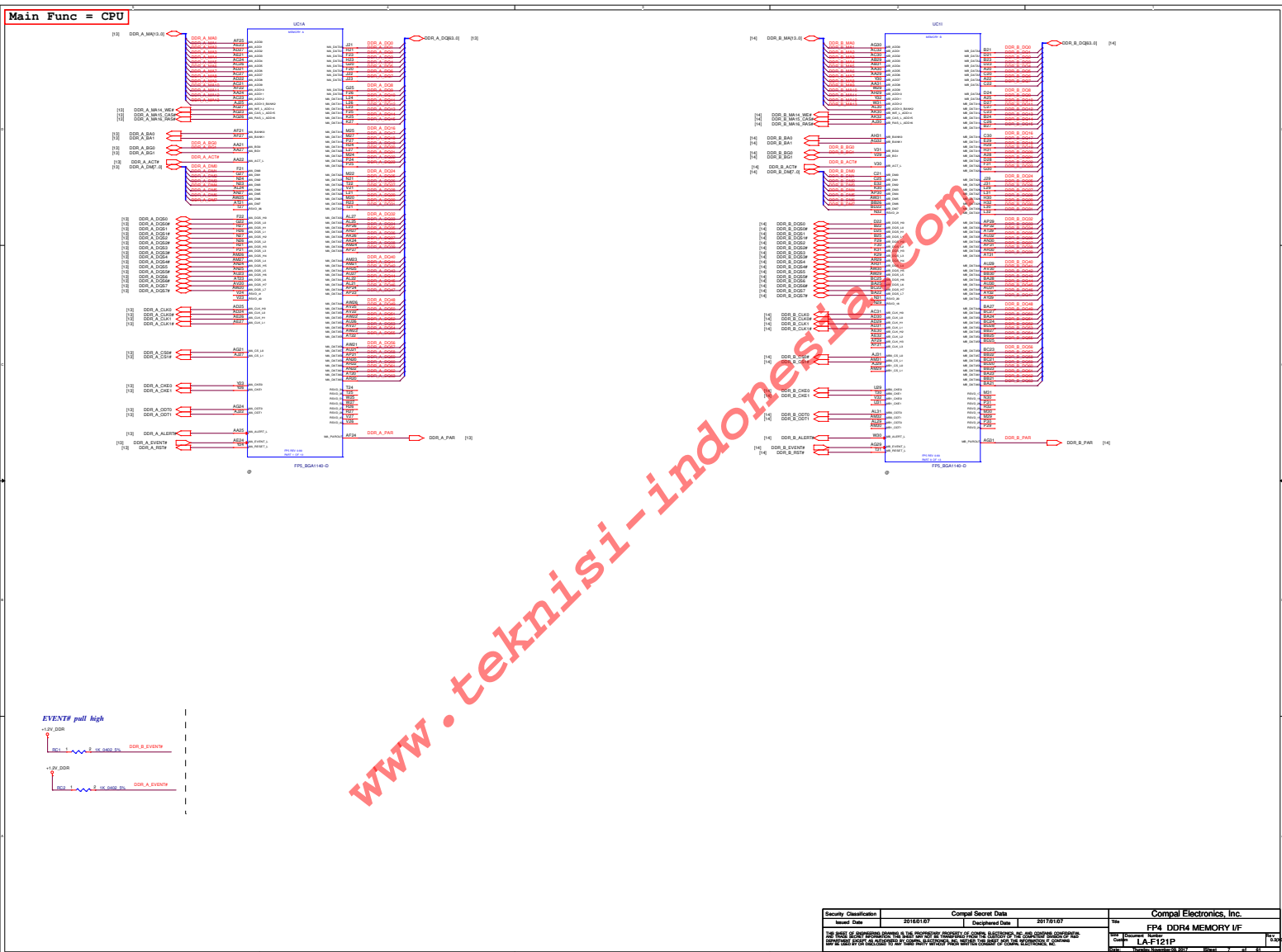
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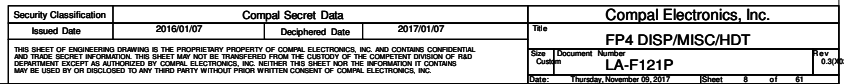
Main Func = CPU

The diagram illustrates the internal connectivity of the Compal F121P laptop. It shows how the main CPU module interfaces with external components like graphics cards (PEG), network adapters (LAN/WLAN), solid state drives (SSD), hard disk drives (HDD), and various control chips (ICs). Each connection is labeled with its respective signal name and pin numbers.

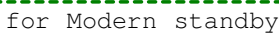
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DP3: TypeC
DP2: CRT
DP1: HDMI
DP0: eDP
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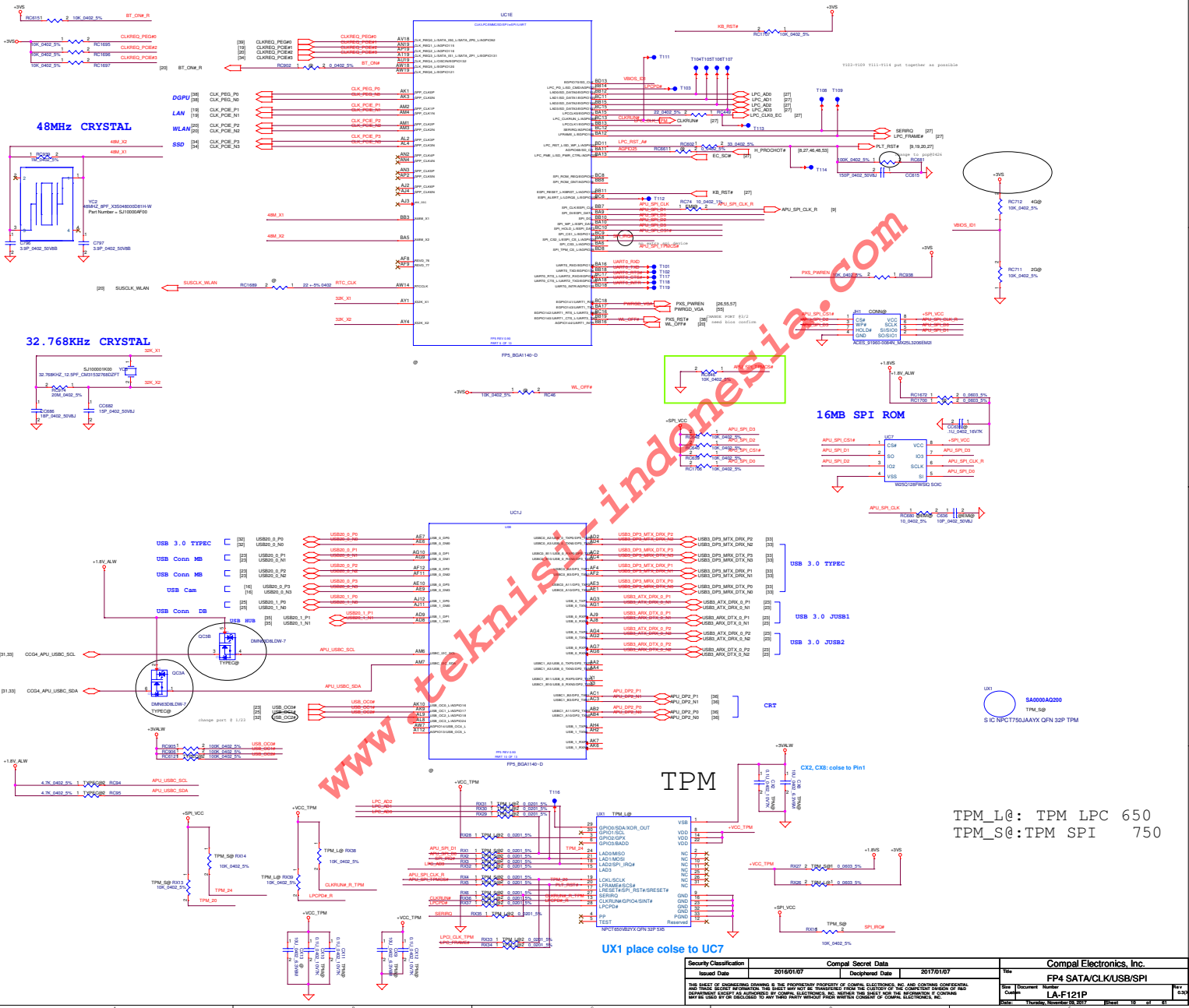


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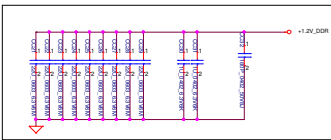
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			<p>Rev. 03/17</p>	

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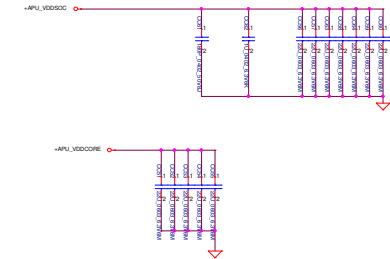
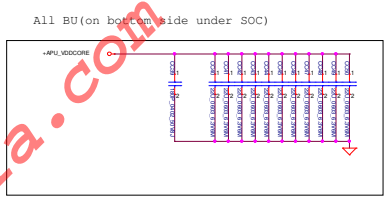
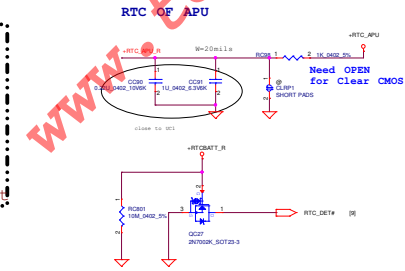
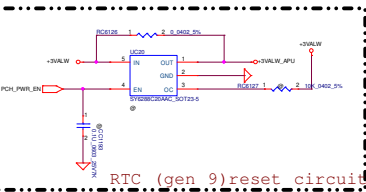
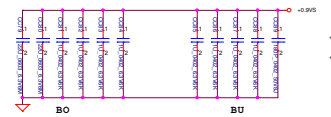
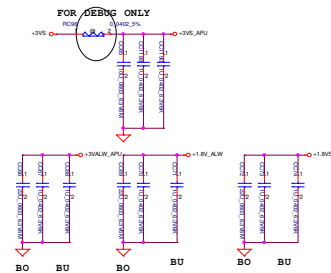
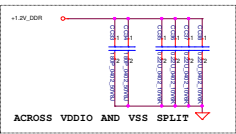


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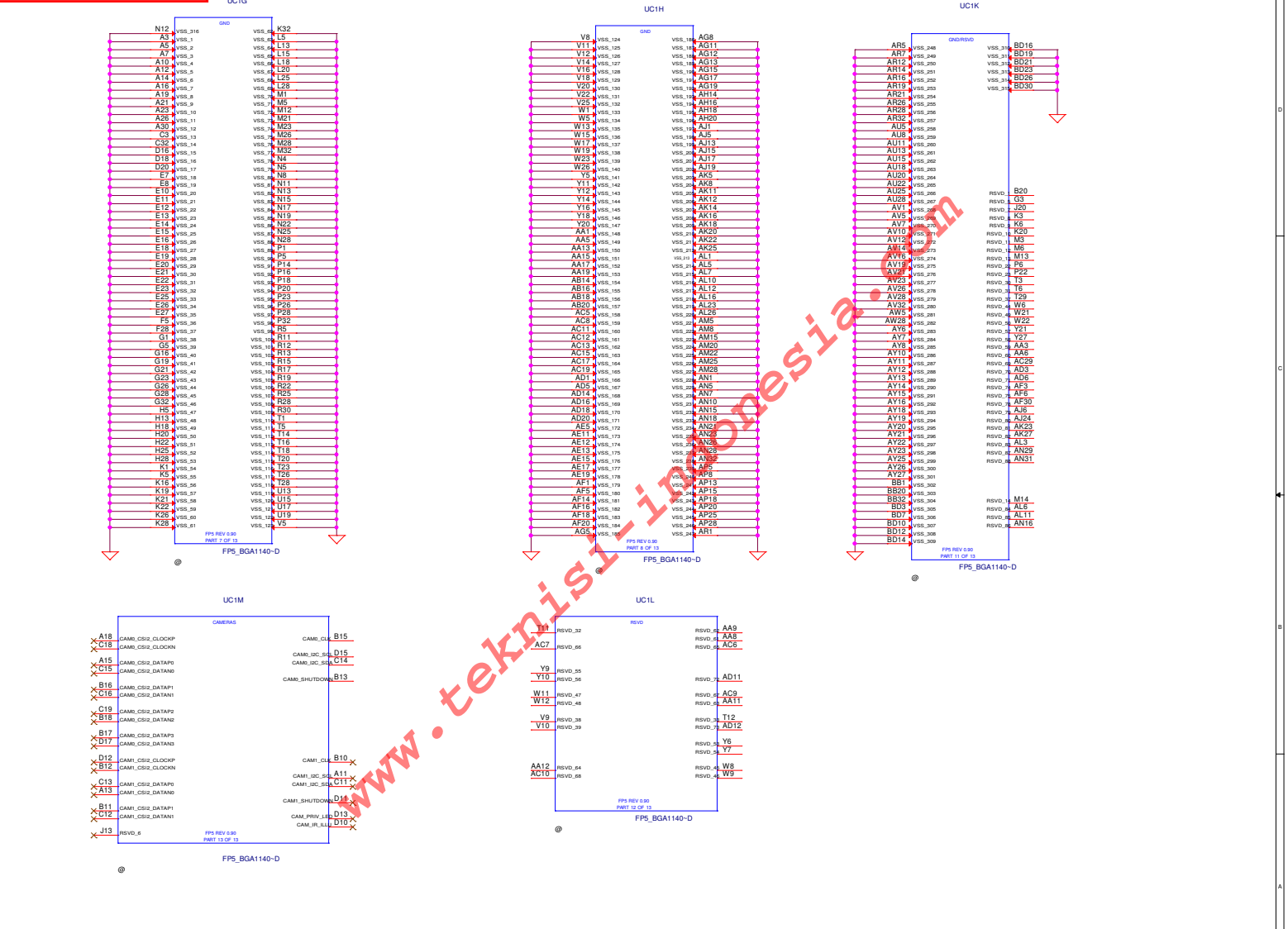


All BU(on bottom side under SOC)



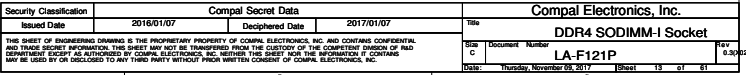
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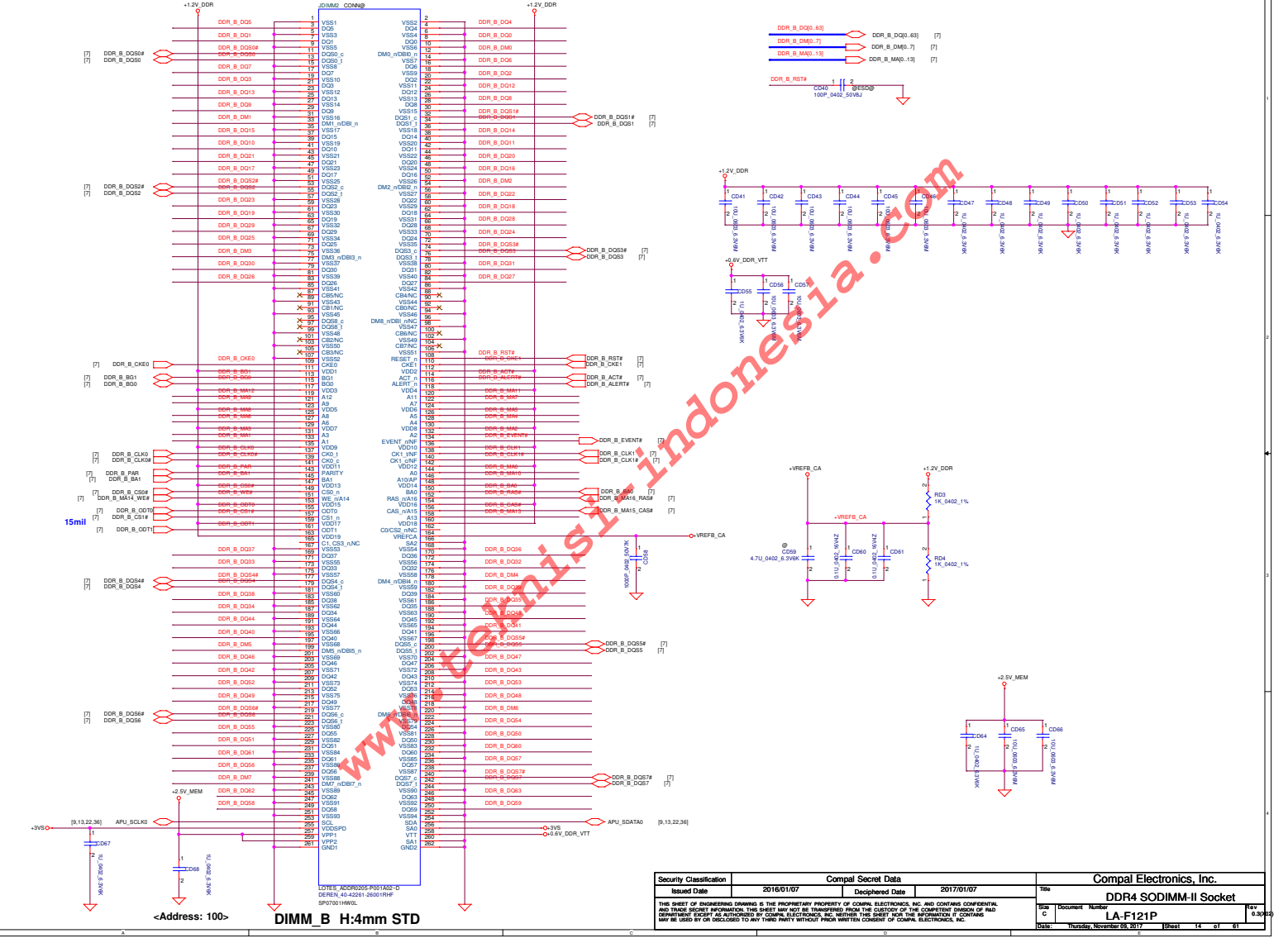


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Main Func = DIMM1

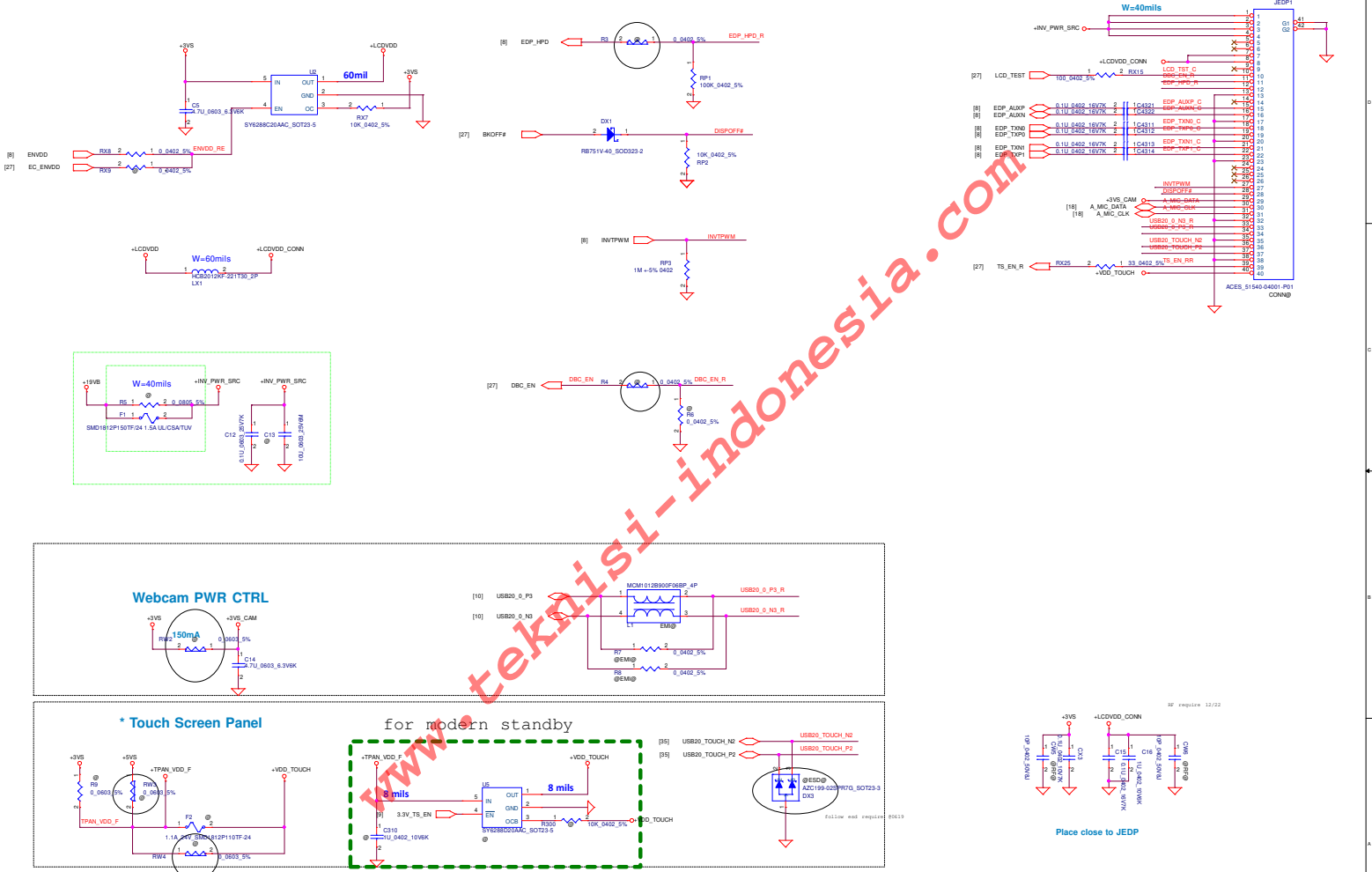


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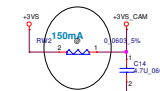


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				LA-F121P	
				Version	
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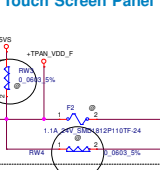
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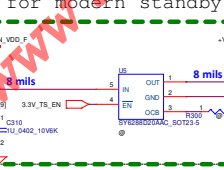
Webcam PWR CTRL



* Touch Screen Panel

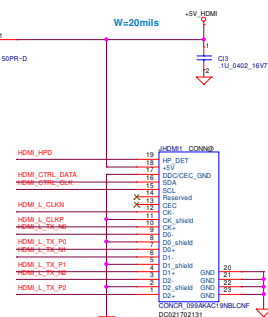
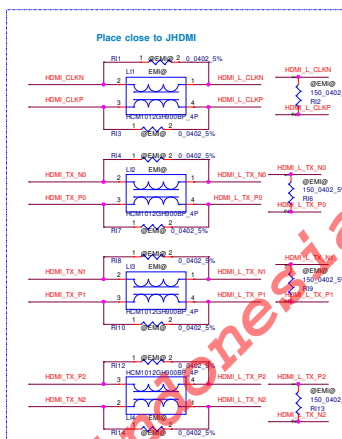
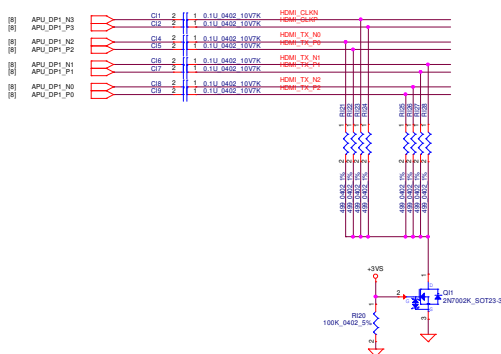


for modern standby

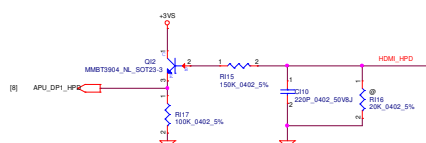
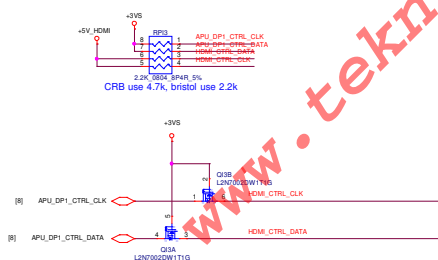


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Main Func = HDMI

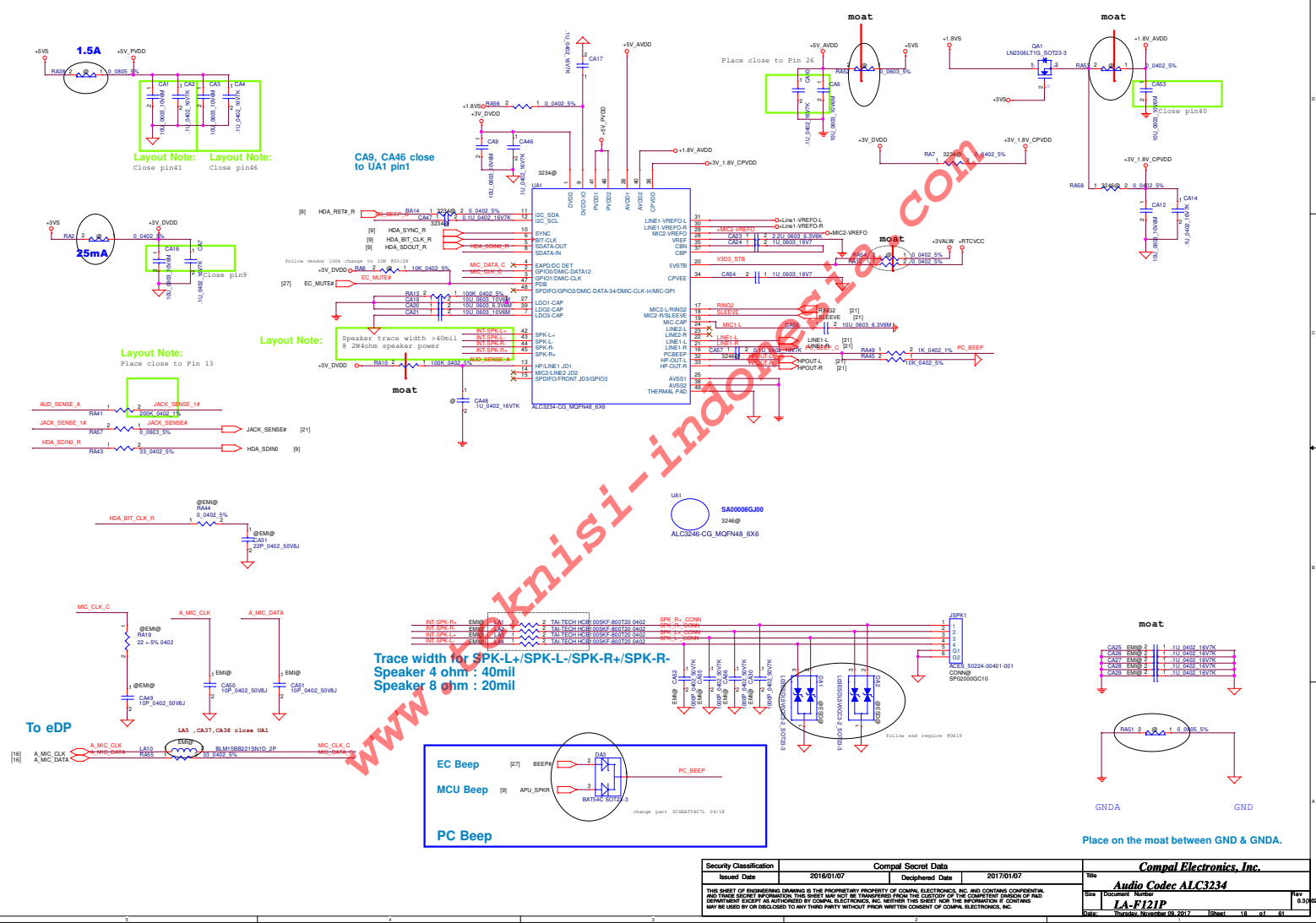


Part Number	Description
800000002HM	HDMI W/Logo:800000002HM



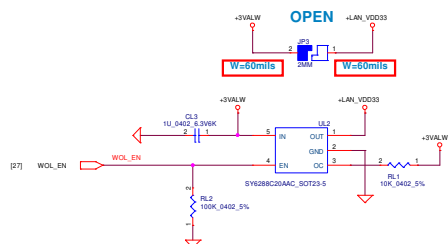
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Main Func = Audio

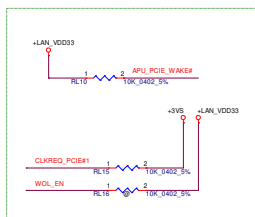
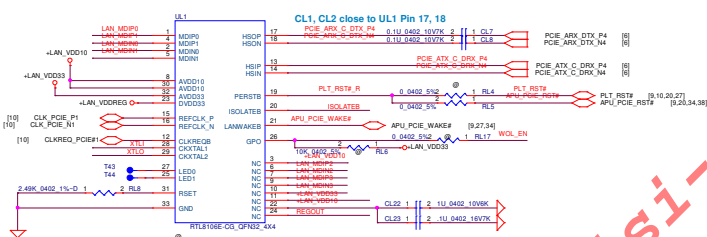


Main Func = LAN

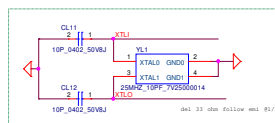
+LAN_VDD33 rising time(10%~90%) : >0.5ms and <100ms



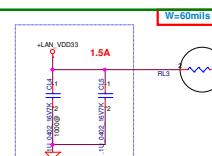
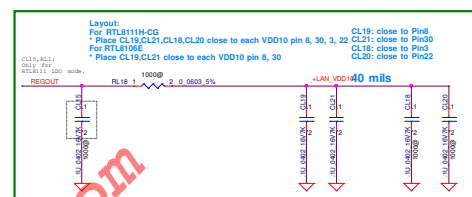
LAN power Noise +LAN_VDD33 < 200mV Vpeak to Vpeak.
LAN power Noise +LAN_VDD10 < 100mV Vpeak to Vpeak.



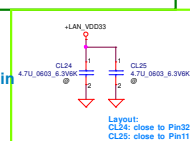
Reserve 10K pull LAN_IO



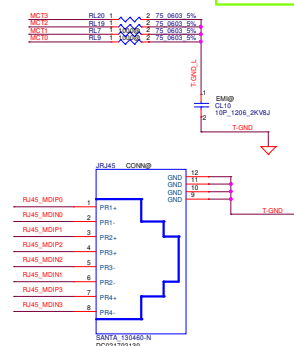
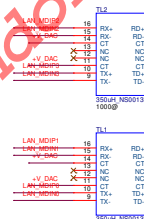
XTAL



Layout:
For RTL8111H-CG
* Place CL4 and CL5 and CL6 close to each VDD33 pin 11, 32, 23
For RTL8106E
* Place CL5 and CL6 close to each VDD33 pin 23, 32



Place close to TCT pi



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Drawn	Document Number	Date		Rev
	IA-F121P	2016.01.07		0.01

Main Func = WLAN

CHANGE WLAN NET NAME 82/23

NGFF WL Con (A Key)

closed to pin 2, 4

+3VS TO +3VS_WLAN_NGFF

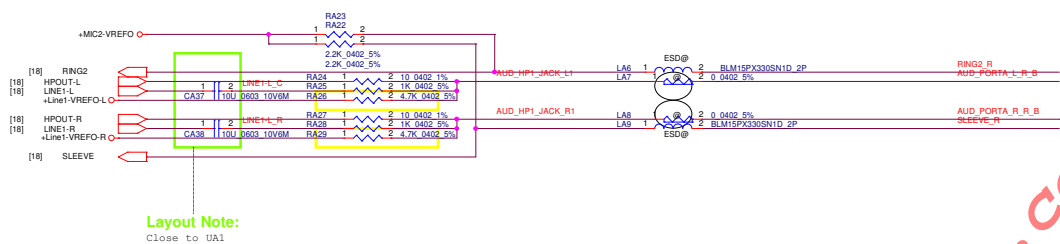
Prevent Backdriver from +3VS_WLAN_NGFF to +3VS

High Active

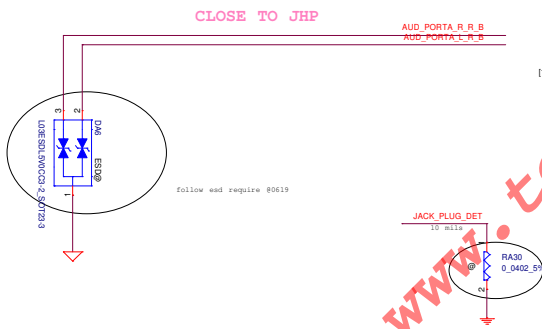
for modern standby

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2016/01/07		2017/01/07		NGFF WLAN	
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				LA-FI21P	030002
				Date: Thursday, November 09, 2017	Sheet 20 of 61

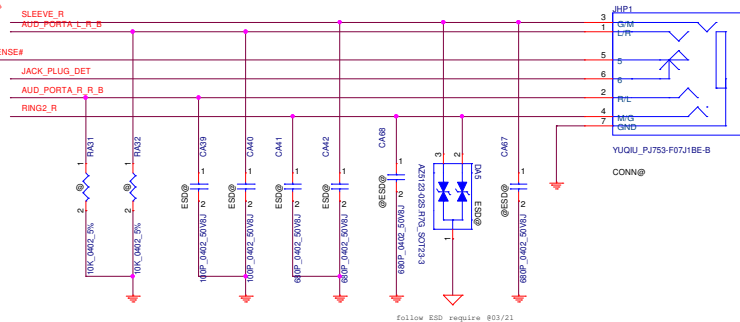
Main Func = Audio Jack



Layout Note:
Close to UA1

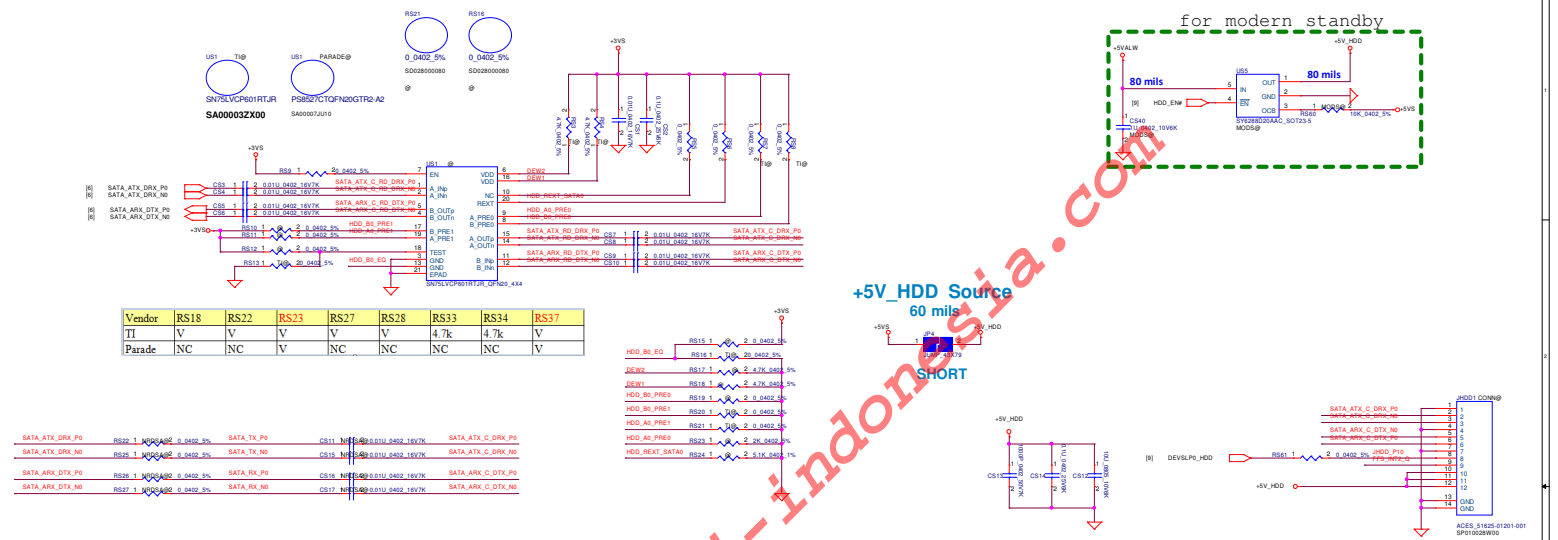


Universal Jack
(Global Headset Jack + mic phone in + line in support)

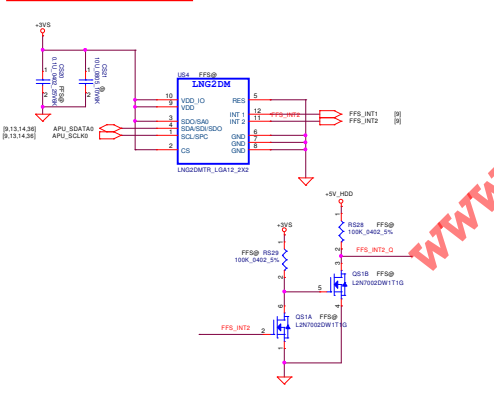


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Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title	JACK
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				Date:	Thursday, November 09, 2017
				Sheet	21 of 61
				Rev	0.3/002

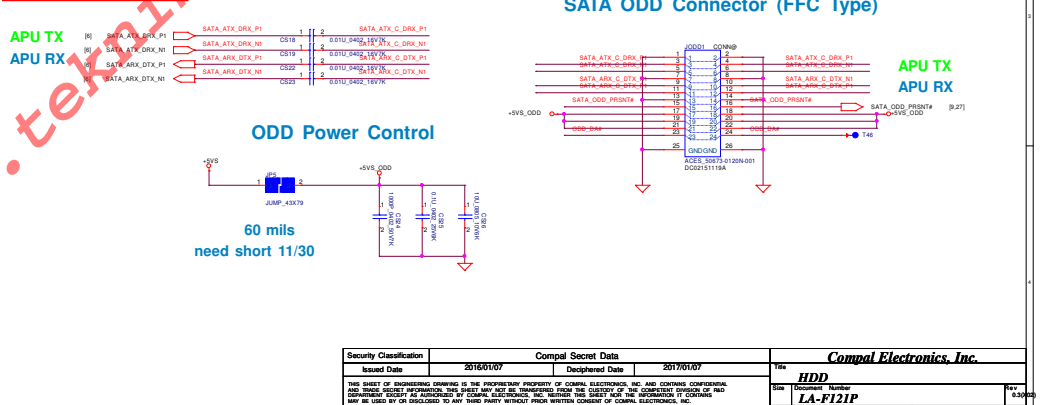
Main Func = HDD



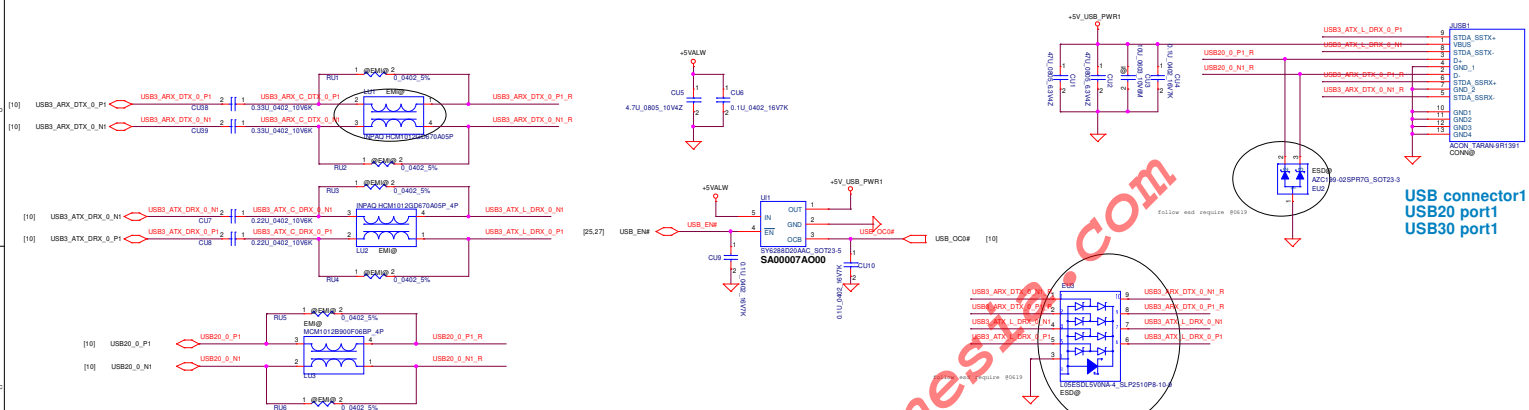
Main Func = FFS



Main Func = ODD

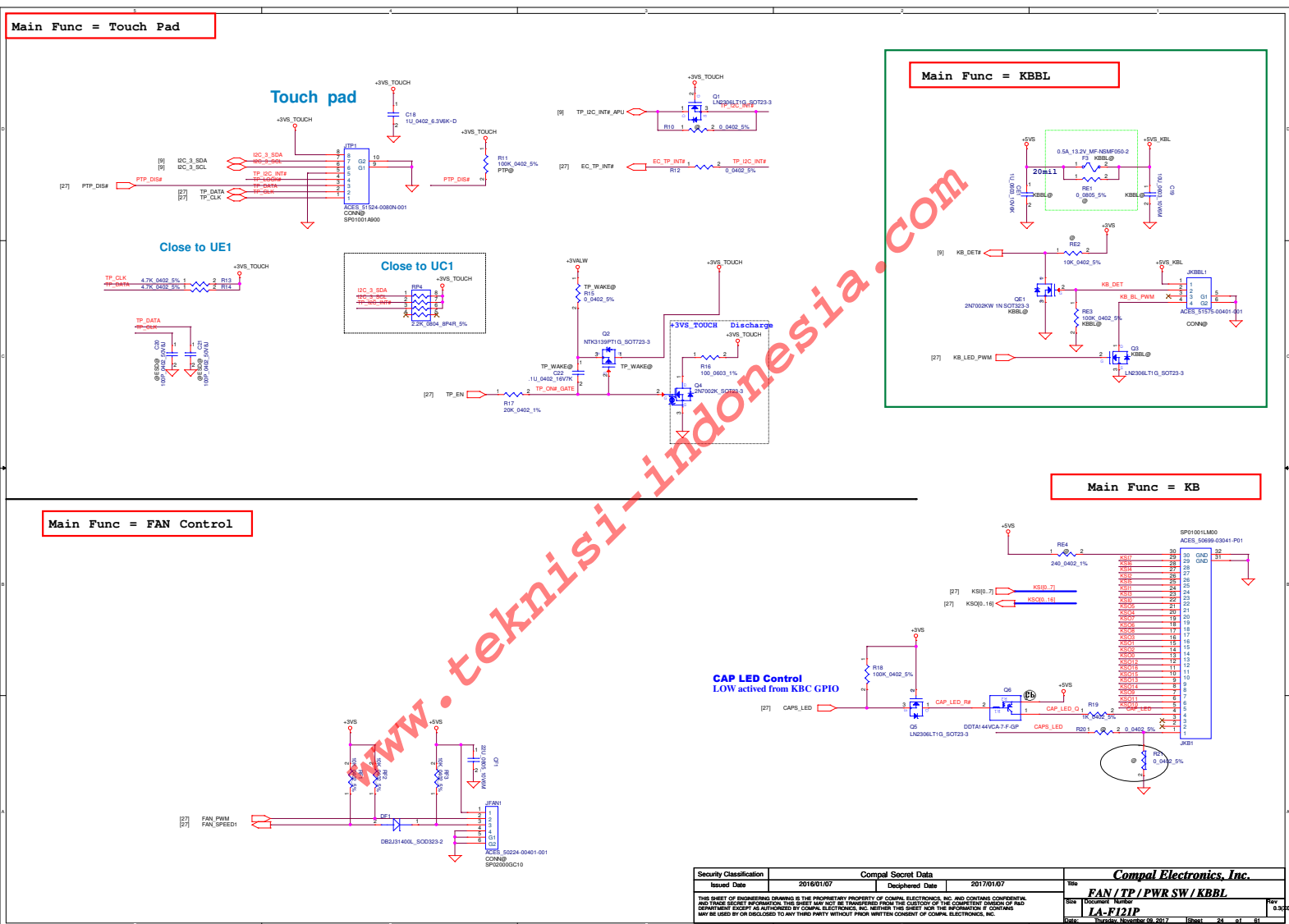


Main Func = USB3.0 Port1



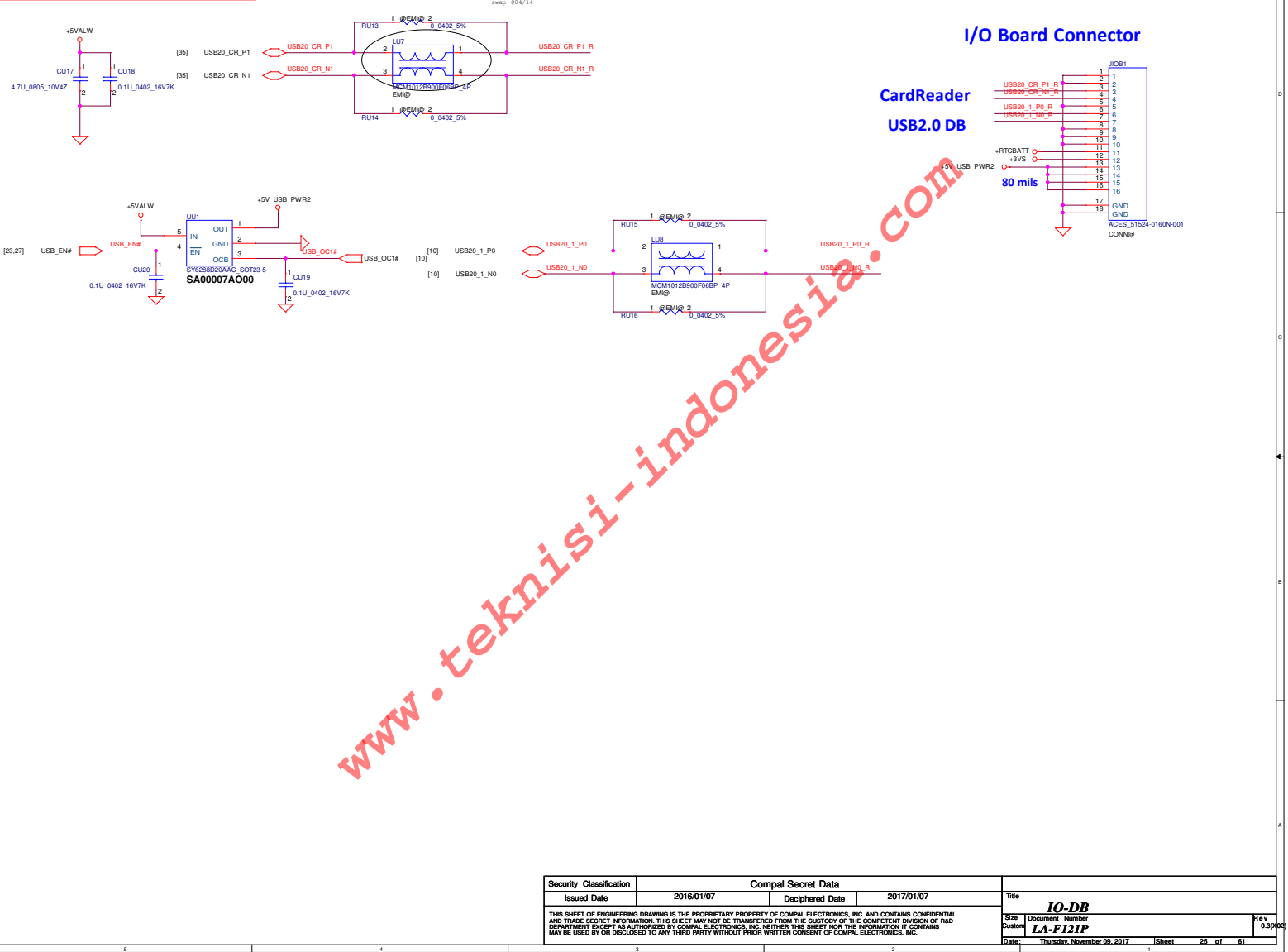
Main Func = USB3.0 Port2

[illegible]



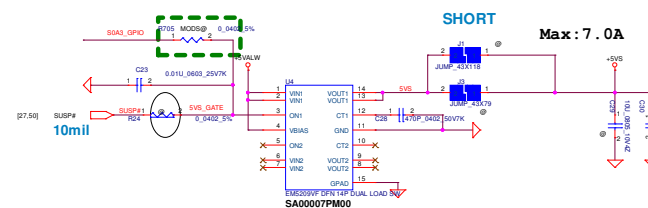
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			Size 100mm X 150mm X 20mm	Date 2017/01/07

Main Func = IO Connector

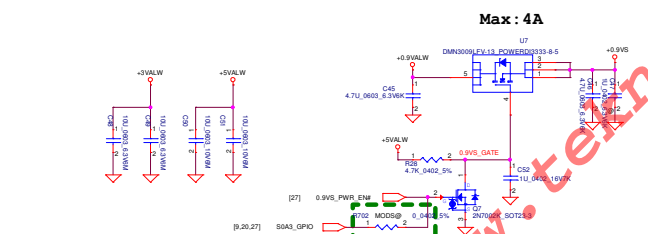
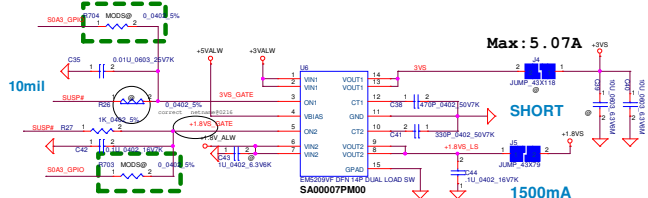
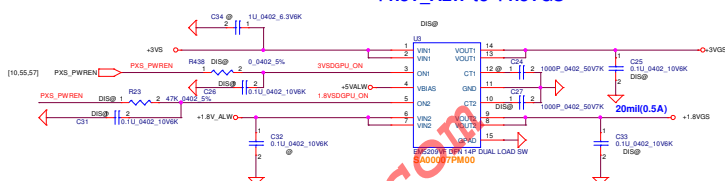


Main Func = DC Interface

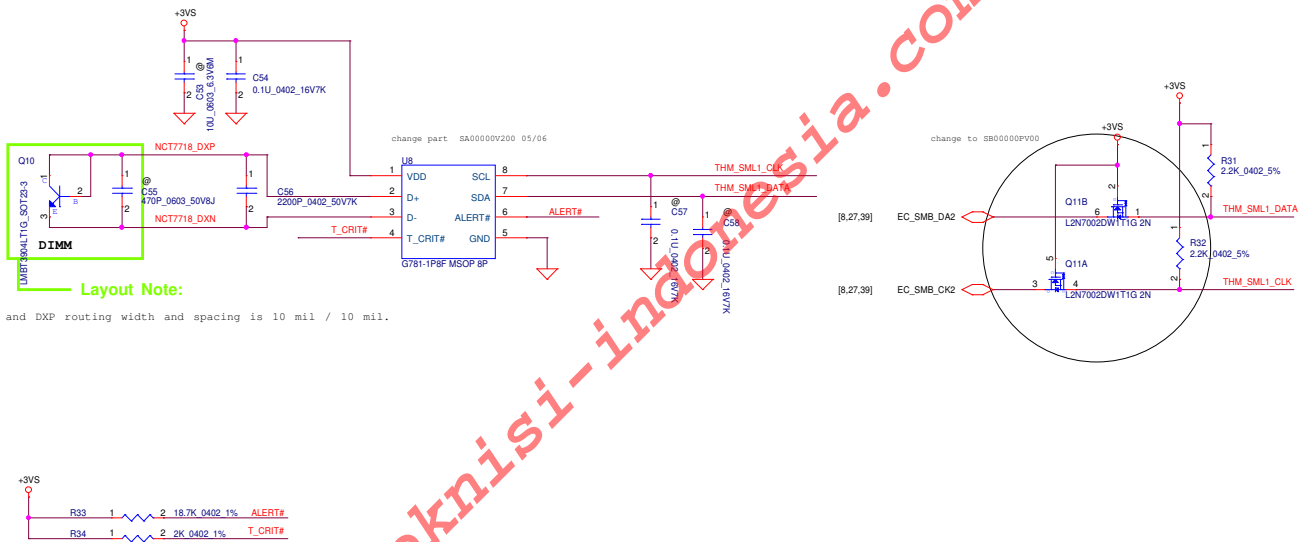
+5VS and +3VS switch



+3VS to +3VGS
+1.8V_ALW to +1.8VGS

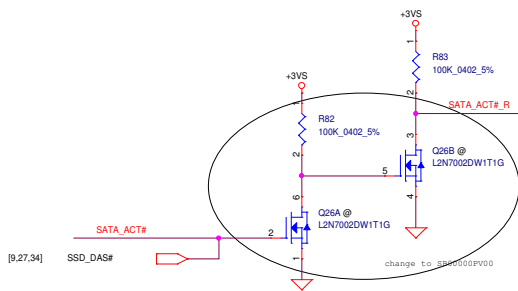


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				LA-F121P	0.01
				Date	Issued
				2016/01/07	2017/01/07

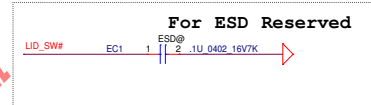
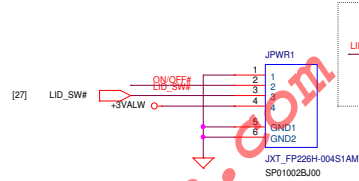


Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title	Thermal Sensor
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				LA-F121P	
				Date: Thursday, November 09, 2017	Sheet 28 of 61

Main Func = POWER BTN



Power button



Pop only before MP

ON/OFF switch

TOP Side

BOT Side

SW1

SW2

S TACT SW TST71A-N-220-S017 SPST H0

S TACT SW TST71A-N-220-S017 SPST H0

ESD@

ESD@

ESD@

ESD@

ESD@

ESD@

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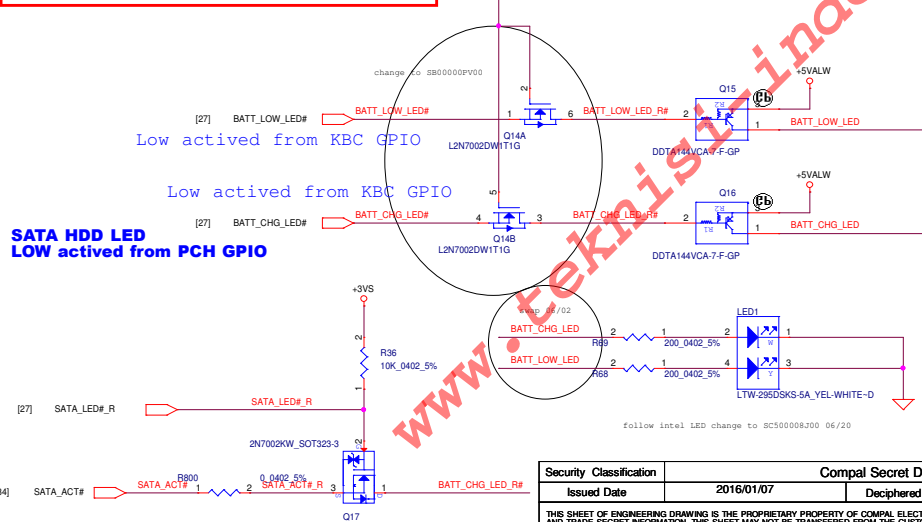
ESD@

ESD@

ESD@

ESD@

Main Func = LED



Security Classification	Compal Secret Data
Issued Date	2016/01/07
Deciphered Date	2017/01/07

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Compal Electronics, Inc.

LED/PWR-DB

Size Document Number

LA-F121P

Date: Thursday, November 08, 2017

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Rev

0.3/0.2

Part Number	Description
DAZ21000100	PCB CAL51 LA-F121P LS-F114P/F121P/F122P

PCB_R1@

Part Number	Description
DAZ21000102	PCB CAL51 LA-F121P LS-F114P/F121P/F122P TRIPOD A31

PCB_R3Y@

Part Number	Description
DAZ21000101	PCB CAL51 LA-F121P LS-F114P/F121P/F122P GOLD A31 !

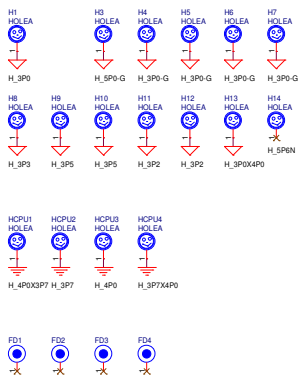
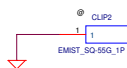
PCB F3G@

ZZZ3

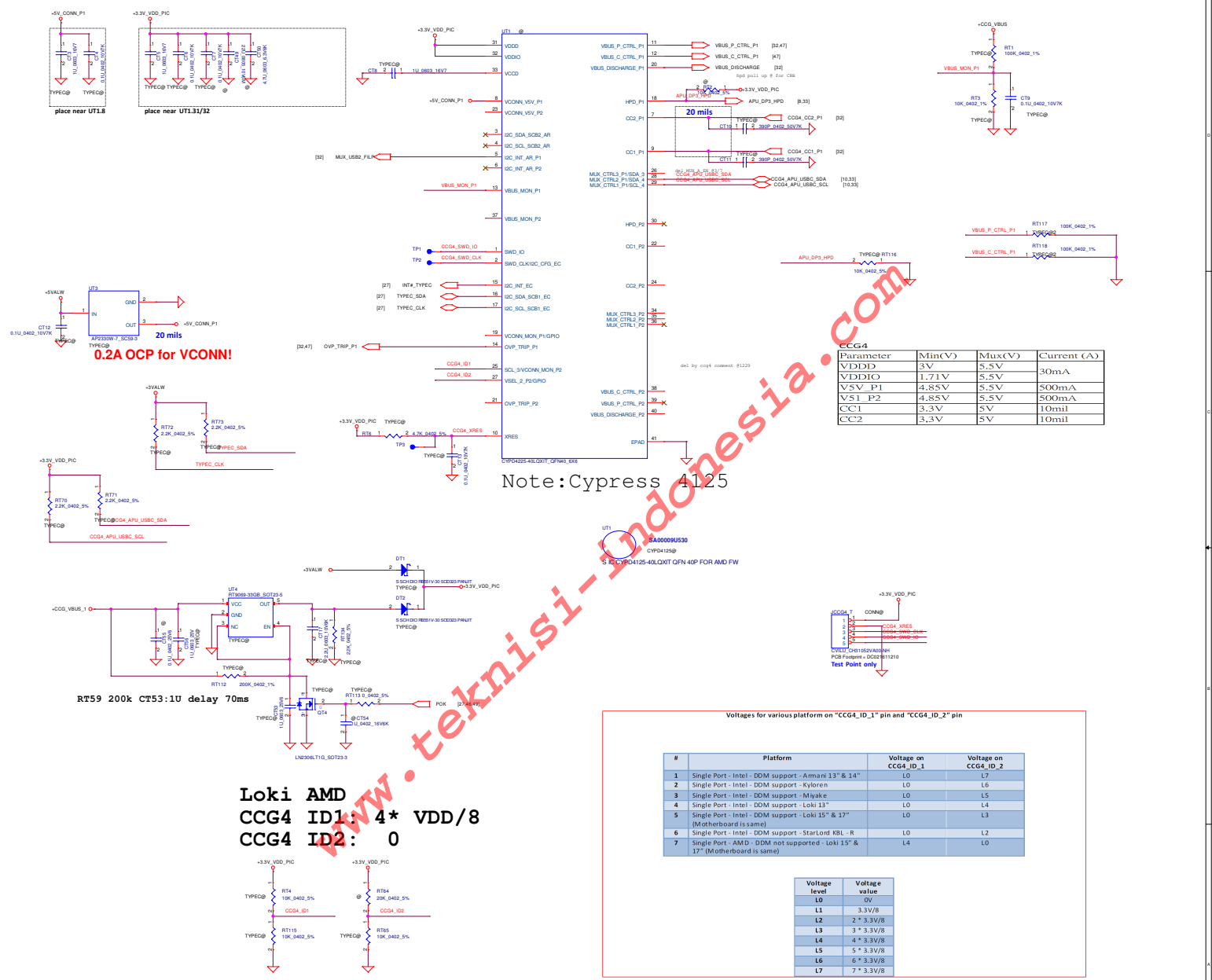
Part Number	Description
DAZ21000104	PCB CAL51 LA-F121P LS-F114P/F121P/F122P T-MAC A31 !

PCB R3H@

del clip1 @04/24

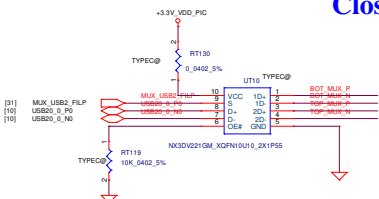


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Date: Thursday, November 09, 2017				Sheet	30	of 35

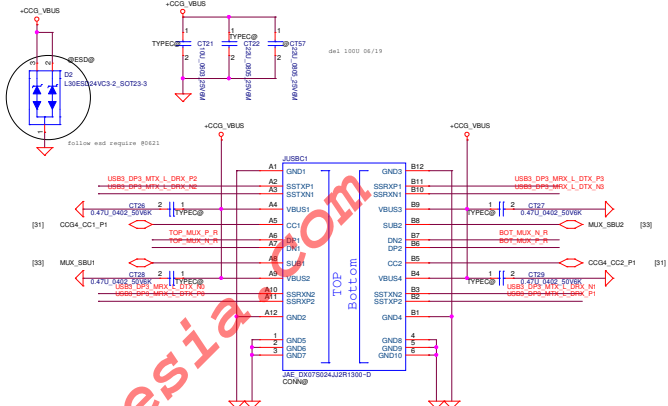
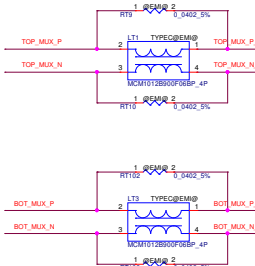


Main Func = USB2 Mux

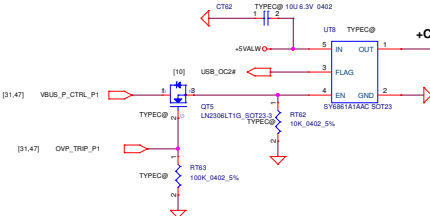
Close to JUSBC1 <500mil



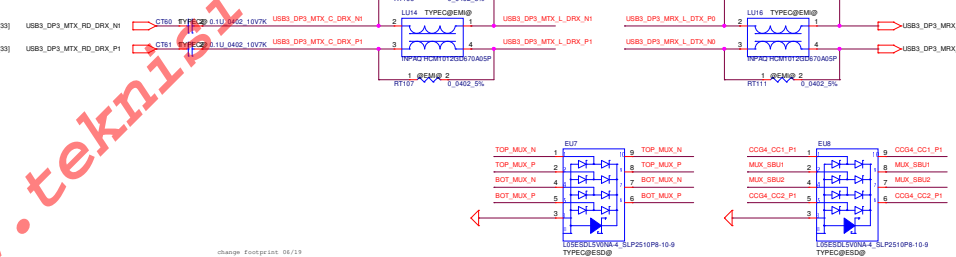
S	OE#	OUT PUT
Low	Low	1D+1D-
High	Low	2D+2D-



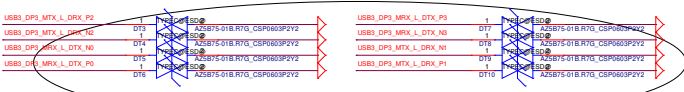
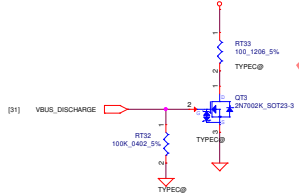
5V@3A



+CCG_VBUS



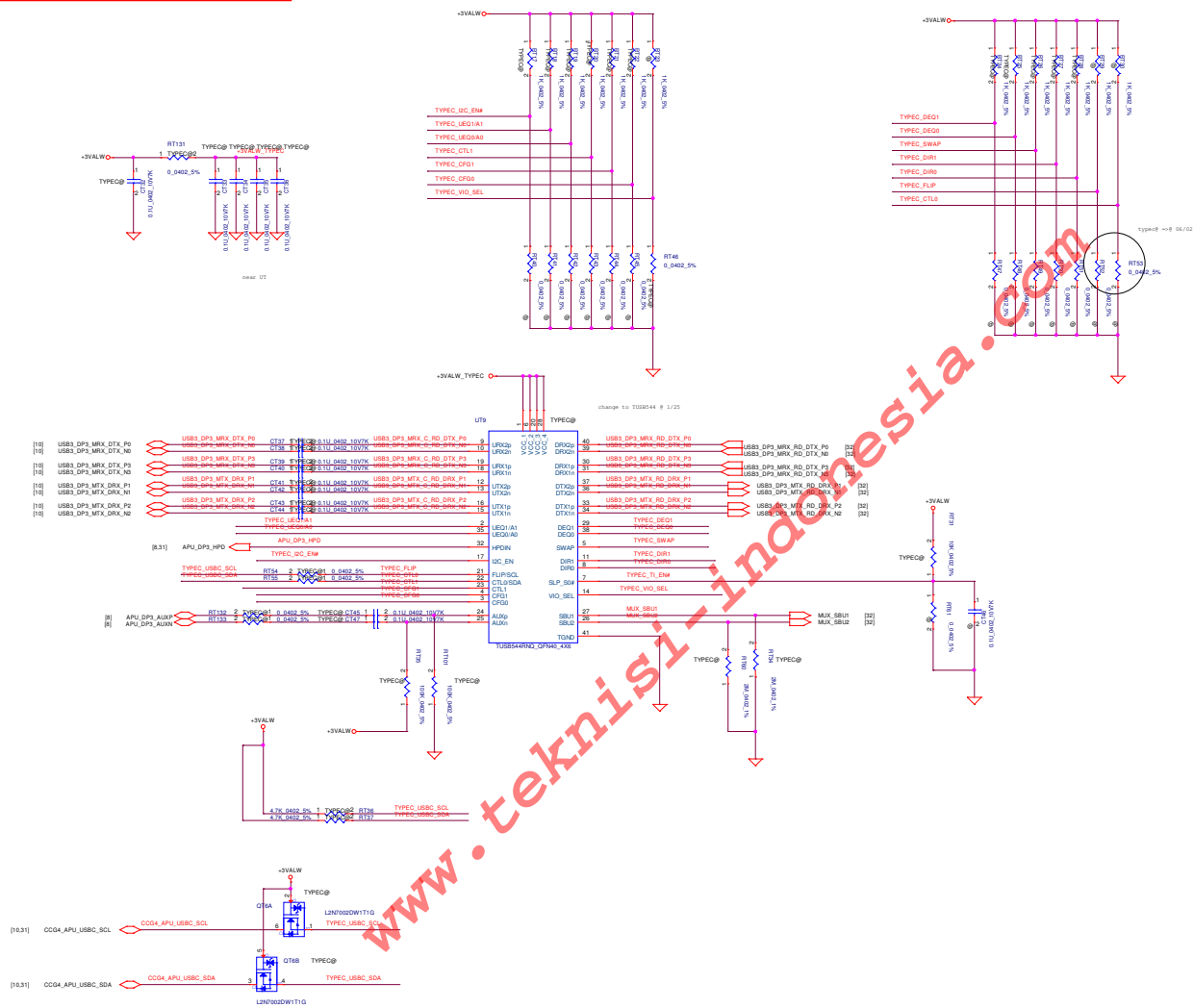
+CCG_VBUS



Type-C 5V Provide Path Control

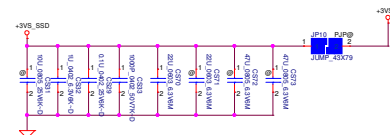
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				LA-F121P		
				Date	Thursday, 09/05/2017	[Sheet 32 of 81]

Main Func = TYPEC Re-driver



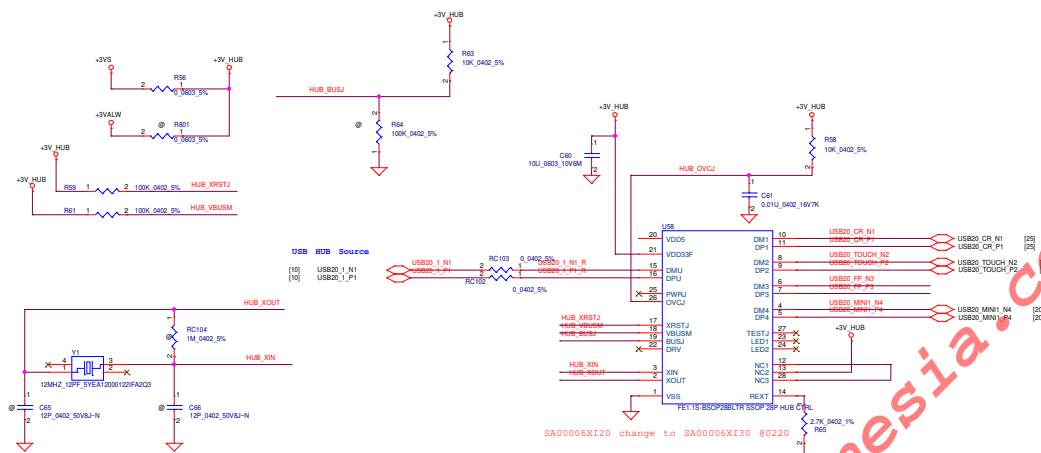
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Main Func = SSD

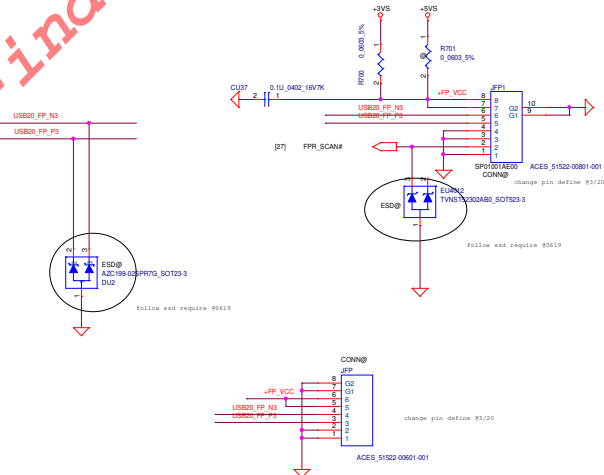


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Date	10/19/2016	Rev	0.0000	

Main Func = USB HUB

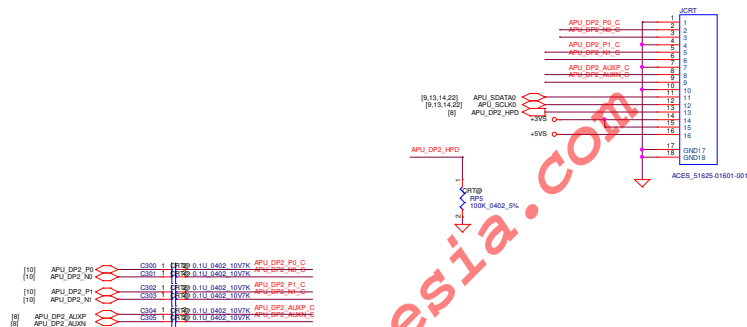


Finger Printer

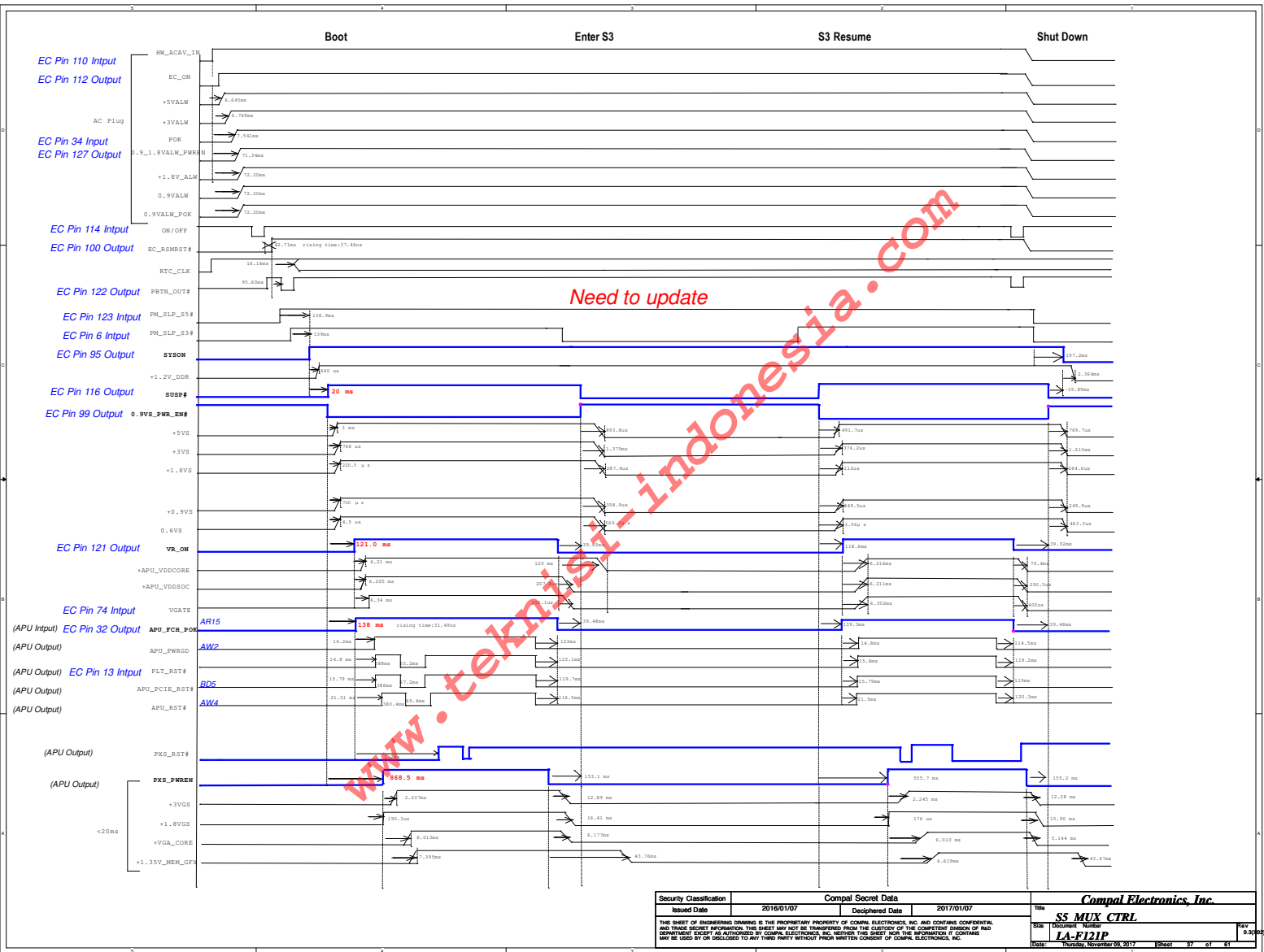


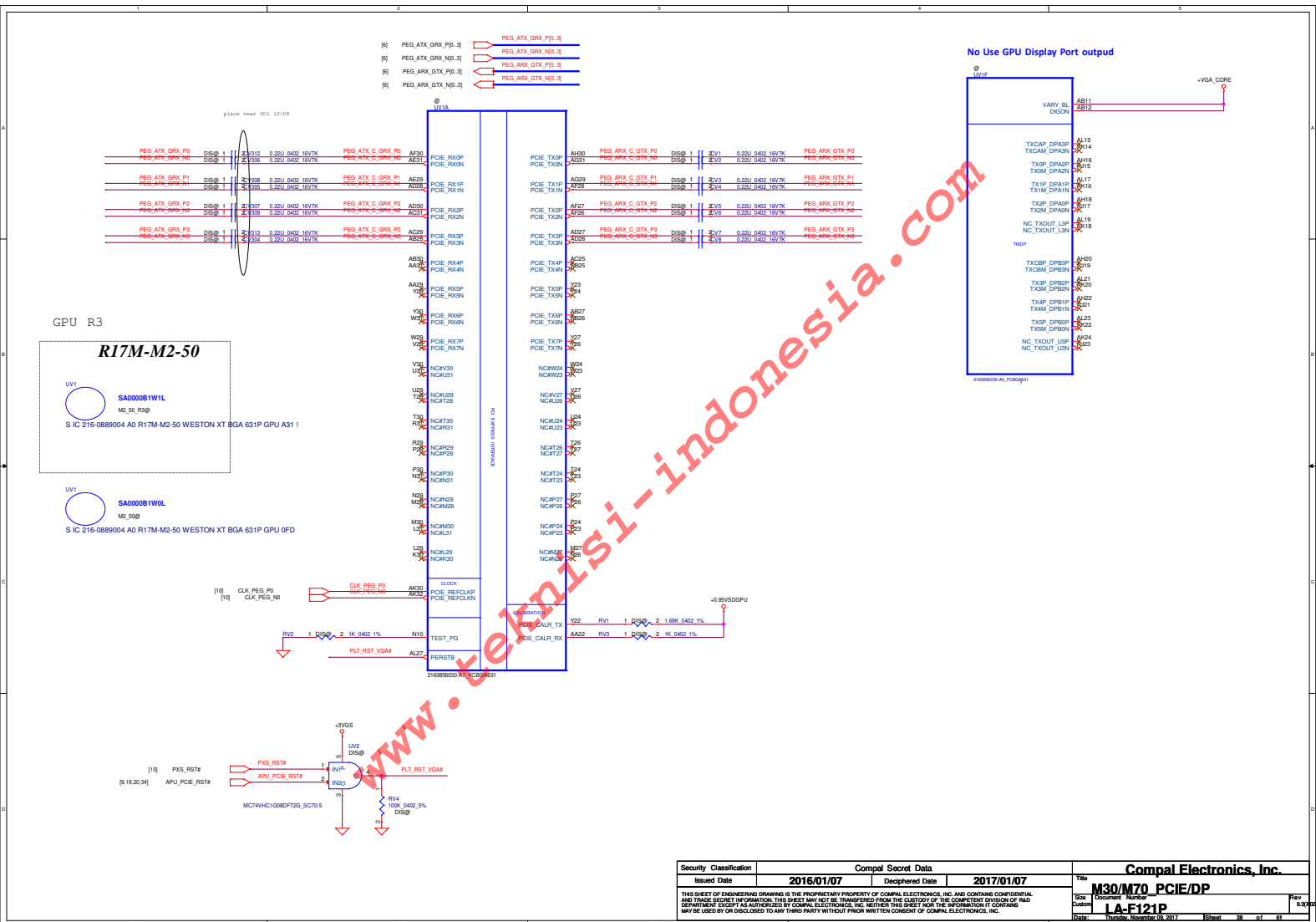
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Issued Date	2014/05/19	Deciphered Date	2015/12/31		
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Date	Thursday, January 09, 2017		Sheet	35	of 61

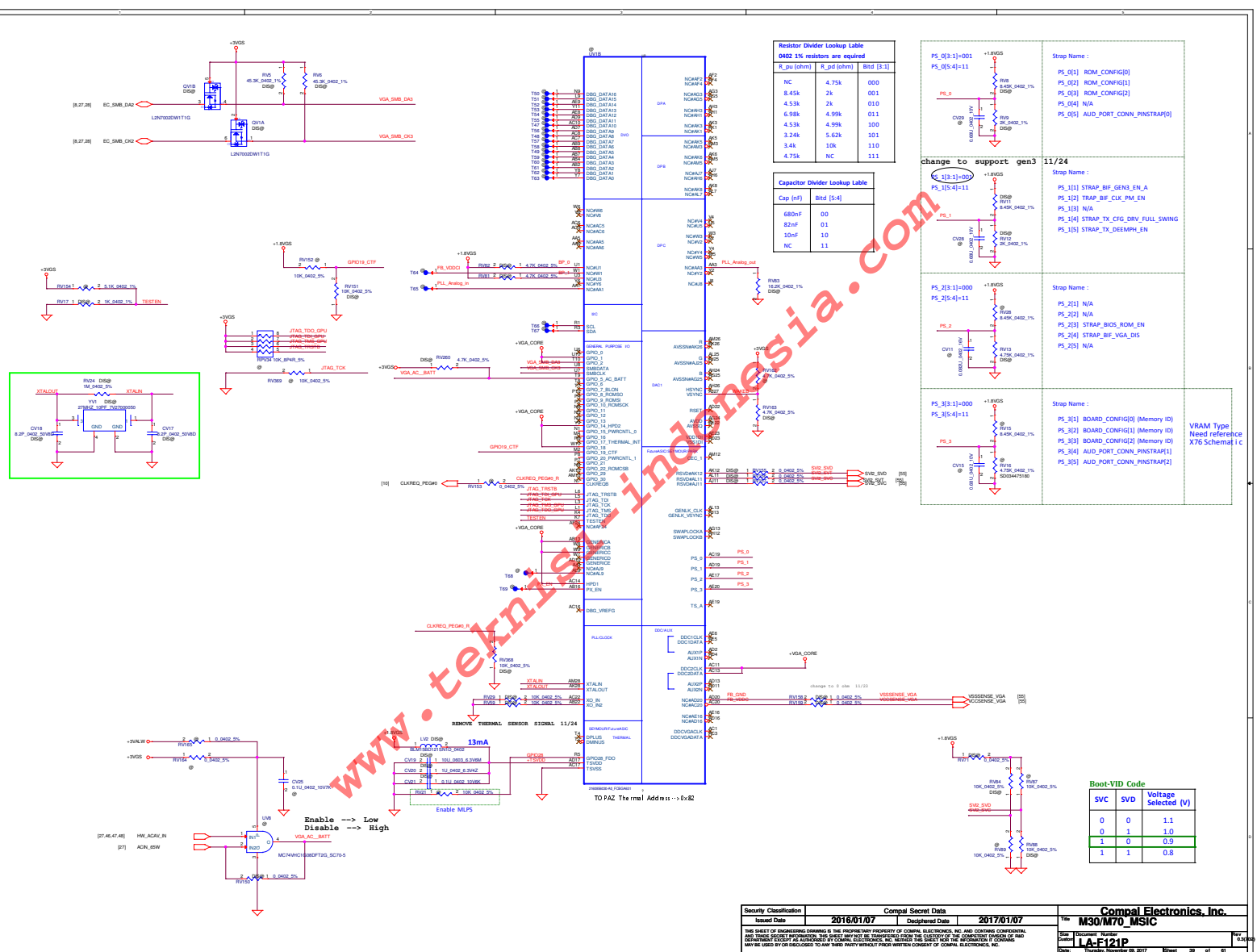
CRT



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Issued Date		Deciphered Date	2017/01/07	Title	Reserve
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Rev	0.00	Docu. Number	LA-F121P	Rev	0.00
Date		Sheet	28	of	61







Resistor Divider Lookup Table			
0402 1% resistors are required			
R _{pu} (ohm)	R _{pd} (ohm)	Brid [3-1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

Capacitor Divider Table	
Cap (nF)	Brid [5-4]
680nF	00
82nF	01
10nF	10
NC	11

PS_0[3:1]=001
PS_0[5:4]=11

change to support gen3
PS_1[3:1]=000
PS_1[5:4]=11

PS_2[3:1]=000
PS_2[5:4]=11

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN

Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A

Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

VRAM Type
Need reference
X76 Schematic

Boot-VID Code		
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Security Classification		Compul Secret Data		Title	
Issued Date		2017/01/07		M30/M70_MSIC	
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Rev		Rev		Rev	
1.0		1.0		1.0	

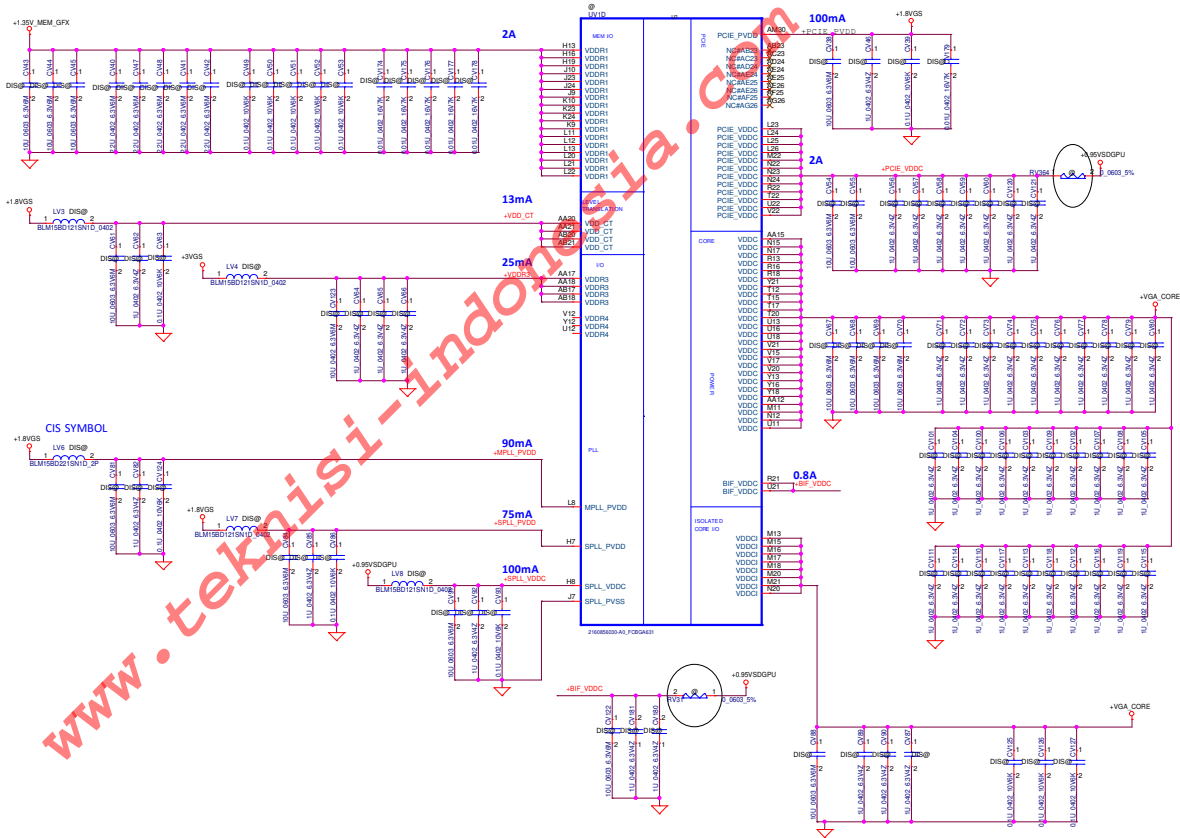
+VGA_CORE		10uF	1uF	0.1uF
VDDC	VDDC_AH6 VDDC1I2 TC2 2A	4	30	0
VDDCI		1	3	3

+0.95VSDGPU		10uF	1uF	0.1uF
PCIE_VDDC	2A	2	7	0
BIF_VDDC	0.8A	1	2	0
SPLL_VDDC	100mA	1	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 2A	3	5	5	5

+1.8VGS		10uF	1uF	0.1uF	0.01uF
PCIE_PVDD	100mA	1	1	1	1
MPLL_PVDD	90mA	1	1	1	0
SPLL_PVDD	75mA	1	1	1	0
VDD_CT	13mA	1	1	1	0
+DP_VDDR	40mA	1(Ⓢ)	1(Ⓢ)	1(Ⓢ)	0
+DP_VDDC		1(Ⓢ)	1(Ⓢ)	1(Ⓢ)	0

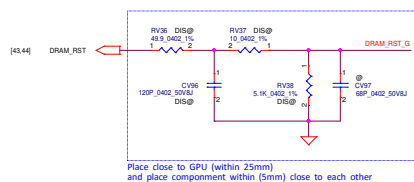
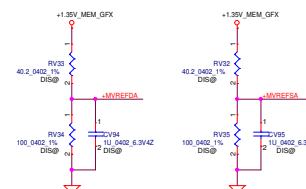
+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	1	3	0



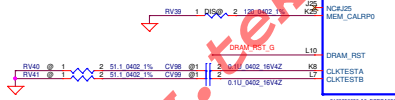
Security Classification	Compel Secret Data		Compel Electronics, Inc.	
Issued Date	2016/01/07	Deciphered Date	2017/01/07	
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Rev	Customer	Title		Rev
		M30/M70 Power		0.0009
		LA-F121P		
		Date: Thursday, November 03, 2017		Release: 41 47 41

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[43.44] M_DA[63..0] M_DA[63..0]
[45] M0_MA[63..0] M0_MA[63..0]
[46] M1_MA[63..0] M1_MA[63..0]

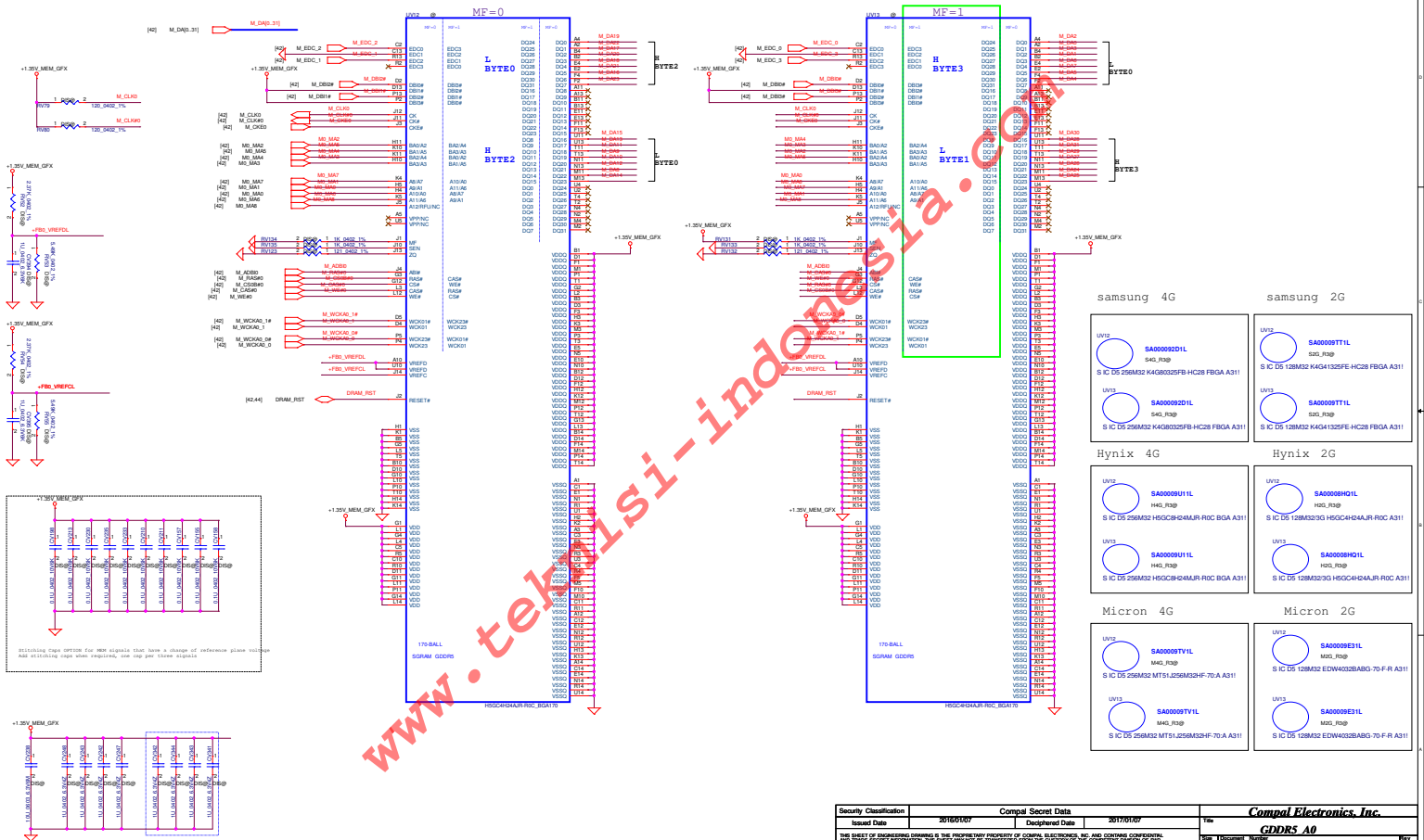


Place close to GPU (within 25mm)
and place component within (5mm) close to each other



M_DAG		M_DAG1		M_DAG2		M_DAG3		M_DAG4		M_DAG5		M_DAG6		M_DAG7		M_DAG8		M_DAG9		M_DAG10		M_DAG11		M_DAG12		M_DAG13		M_DAG14		M_DAG15		M_DAG16		M_DAG17		M_DAG18		M_DAG19		M_DAG20		M_DAG21		M_DAG22		M_DAG23		M_DAG24		M_DAG25		M_DAG26		M_DAG27		M_DAG28		M_DAG29		M_DAG30		M_DAG31		M_DAG32		M_DAG33		M_DAG34		M_DAG35		M_DAG36		M_DAG37		M_DAG38		M_DAG39		M_DAG40		M_DAG41		M_DAG42		M_DAG43		M_DAG44		M_DAG45		M_DAG46		M_DAG47		M_DAG48		M_DAG49		M_DAG50		M_DAG51		M_DAG52		M_DAG53		M_DAG54		M_DAG55		M_DAG56		M_DAG57		M_DAG58		M_DAG59		M_DAG60		M_DAG61		M_DAG62		M_DAG63		M_DAG64		M_DAG65		M_DAG66		M_DAG67		M_DAG68		M_DAG69		M_DAG70		M_DAG71		M_DAG72		M_DAG73		M_DAG74		M_DAG75		M_DAG76		M_DAG77		M_DAG78		M_DAG79		M_DAG80		M_DAG81		M_DAG82		M_DAG83		M_DAG84		M_DAG85		M_DAG86		M_DAG87		M_DAG88		M_DAG89		M_DAG90		M_DAG91		M_DAG92		M_DAG93		M_DAG94		M_DAG95		M_DAG96		M_DAG97		M_DAG98		M_DAG99		M_DAG100		M_DAG101		M_DAG102		M_DAG103		M_DAG104		M_DAG105		M_DAG106		M_DAG107		M_DAG108		M_DAG109		M_DAG110		M_DAG111		M_DAG112		M_DAG113		M_DAG114		M_DAG115		M_DAG116		M_DAG117		M_DAG118		M_DAG119		M_DAG120		M_DAG121		M_DAG122		M_DAG123		M_DAG124		M_DAG125		M_DAG126		M_DAG127		M_DAG128		M_DAG129		M_DAG130		M_DAG131		M_DAG132		M_DAG133		M_DAG134		M_DAG135		M_DAG136		M_DAG137		M_DAG138		M_DAG139		M_DAG140		M_DAG141		M_DAG142		M_DAG143		M_DAG144		M_DAG145		M_DAG146		M_DAG147		M_DAG148		M_DAG149		M_DAG150		M_DAG151		M_DAG152		M_DAG153		M_DAG154		M_DAG155		M_DAG156		M_DAG157		M_DAG158		M_DAG159		M_DAG160		M_DAG161		M_DAG162		M_DAG163		M_DAG164		M_DAG165		M_DAG166		M_DAG167		M_DAG168		M_DAG169		M_DAG170		M_DAG171		M_DAG172		M_DAG173		M_DAG174		M_DAG175		M_DAG176		M_DAG177		M_DAG178		M_DAG179		M_DAG180		M_DAG181		M_DAG182		M_DAG183		M_DAG184		M_DAG185		M_DAG186		M_DAG187		M_DAG188		M_DAG189		M_DAG190		M_DAG191		M_DAG192		M_DAG193		M_DAG194		M_DAG195		M_DAG196		M_DAG197		M_DAG198		M_DAG199		M_DAG200		M_DAG201		M_DAG202		M_DAG203		M_DAG204		M_DAG205		M_DAG206		M_DAG207		M_DAG208		M_DAG209		M_DAG210		M_DAG211		M_DAG212		M_DAG213		M_DAG214		M_DAG215		M_DAG216		M_DAG217		M_DAG218		M_DAG219		M_DAG220		M_DAG221		M_DAG222		M_DAG223		M_DAG224		M_DAG225		M_DAG226		M_DAG227		M_DAG228		M_DAG229		M_DAG230		M_DAG231		M_DAG232		M_DAG233		M_DAG234		M_DAG235		M_DAG236		M_DAG237		M_DAG238		M_DAG239		M_DAG240		M_DAG241		M_DAG242		M_DAG243		M_DAG244		M_DAG245		M_DAG246		M_DAG247		M_DAG248		M_DAG249		M_DAG250		M_DAG251		M_DAG252		M_DAG253		M_DAG254		M_DAG255		M_DAG256		M_DAG257		M_DAG258		M_DAG259		M_DAG260		M_DAG261		M_DAG262		M_DAG263		M_DAG264		M_DAG265		M_DAG266		M_DAG267		M_DAG268		M_DAG269		M_DAG270		M_DAG271		M_DAG272		M_DAG273		M_DAG274		M_DAG275		M_DAG276		M_DAG277		M_DAG278		M_DAG279		M_DAG280		M_DAG281		M_DAG282		M_DAG283		M_DAG284		M_DAG285		M_DAG286		M_DAG287		M_DAG288		M_DAG289		M_DAG290		M_DAG291		M_DAG292		M_DAG293		M_DAG294		M_DAG295		M_DAG296		M_DAG297		M_DAG298		M_DAG299		M_DAG300		M_DAG301		M_DAG302		M_DAG303		M_DAG304		M_DAG305		M_DAG306		M_DAG307		M_DAG308		M_DAG309		M_DAG310		M_DAG311		M_DAG312		M_DAG313		M_DAG314		M_DAG315		M_DAG316		M_DAG317		M_DAG318		M_DAG319		M_DAG320		M_DAG321		M_DAG322		M_DAG323		M_DAG324		M_DAG325		M_DAG326		M_DAG327		M_DAG328		M_DAG329		M_DAG330		M_DAG331		M_DAG332		M_DAG333		M_DAG334		M_DAG335		M_DAG336		M_DAG337		M_DAG338		M_DAG339		M_DAG340		M_DAG341		M_DAG342		M_DAG343		M_DAG344		M_DAG345		M_DAG346		M_DAG347		M_DAG348		M_DAG349		M_DAG350		M_DAG351		M_DAG352		M_DAG353		M_DAG354		M_DAG355		M_DAG356		M_DAG357		M_DAG358		M_DAG359		M_DAG360		M_DAG361		M_DAG362		M_DAG363		M_DAG364		M_DAG365		M_DAG366		M_DAG367		M_DAG368		M_DAG369		M_DAG370		M_DAG371		M_DAG372		M_DAG373		M_DAG374		M_DAG375		M_DAG376		M_DAG377		M_DAG378		M_DAG379		M_DAG380		M_DAG381		M_DAG382		M_DAG383		M_DAG384		M_DAG385		M_DAG386		M_DAG387		M_DAG388		M_DAG389		M_DAG390		M_DAG391		M_DAG392		M_DAG393		M_DAG394		M_DAG395		M_DAG396		M_DAG397		M_DAG398		M_DAG399		M_DAG400		M_DAG401		M_DAG402		M_DAG403		M_DAG404		M_DAG405		M_DAG406		M_DAG407		M_DAG408		M_DAG409		M_DAG410		M_DAG411		M_DAG412		M_DAG413		M_DAG414		M_DAG415		M_DAG416		M_DAG417		M_DAG418		M_DAG419		M_DAG420		M_DAG421		M_DAG422		M_DAG423		M_DAG424		M_DAG425		M_DAG426		M_DAG427		M_DAG428		M_DAG429		M_DAG430		M_DAG431		M_DAG432		M_DAG433		M_DAG434		M_DAG435		M_DAG436		M_DAG437		M_DAG438		M_DAG439		M_DAG440		M_DAG441		M_DAG442		M_DAG443		M_DAG444		M_DAG445		M_DAG446		M_DAG447		M_DAG448		M_DAG449		M_DAG450		M_DAG451		M_DAG452		M_DAG453		M_DAG454		M_DAG455		M_DAG456		M_DAG457		M_DAG458		M_DAG459		M_DAG460		M_DAG461		M_DAG462		M_DAG463		M_DAG464		M_DAG465		M_DAG466		M_DAG467		M_DAG468		M_DAG469		M_DAG470		M_DAG471		M_DAG472		M_DAG473		M_DAG474		M_DAG475		M_DAG476		M_DAG477		M_DAG478		M_DAG479		M_DAG480		M_DAG481		M_DAG482		M_DAG483		M_DAG484		M_DAG485		M_DAG486		M_DAG487		M_DAG488		M_DAG489		M_DAG490		M_DAG491		M_DAG492		M_DAG493		M_DAG494		M_DAG495		M_DAG496		M_DAG497		M_DAG498		M_DAG499		M_DAG500		M_DAG501		M_DAG502		M_DAG503		M_DAG504		M_DAG505		M_DAG506		M_DAG507		M_DAG508		M_DAG509		M_DAG510		M_DAG511		M_DAG512		M_DAG513		M_DAG514		M_DAG515		M_DAG516		M_DAG517		M_DAG518		M_DAG519		M_DAG520		M_DAG521		M_DAG522		M_DAG523		M_DAG524		M_DAG525		M_DAG526		M_DAG527		M_DAG528		M_DAG529		M_DAG530		M_DAG531		M_DAG532		M_DAG533		M_DAG534		M_DAG535		M_DAG536		M_DAG537		M_DAG538		M_DAG539		M_DAG540		M_DAG541		M_DAG542		M_DAG543		M_DAG544		M_DAG545		M_DAG546		M_DAG547		M_DAG548		M_DAG549		M_DAG550		M_DAG551		M_DAG552		M_DAG553		M_DAG554		M_DAG555		M_DAG556		M_DAG557		M_DAG558		M_DAG559		M_DAG560		M_DAG561		M_DAG562		M_DAG563		M_DAG564		M_DAG565		M_DAG566		M_DAG567		M_DAG568		M_DAG569		M_DAG570		M_DAG571		M_DAG572		M_DAG573		M_DAG574		M_DAG575		M_DAG576		M_DAG577		M_DAG578		M_DAG579		M_DAG580		M_DAG581		M_DAG582		M_DAG583		M_DAG584		M_DAG585		M_DAG586		M_DAG587		M_DAG588		M_DAG589		M_DAG590		M_DAG591		M_DAG592		M_DAG593		M_DAG594		M_DAG595		M_DAG596		M_DAG597		M_DAG598		M_DAG599		M_DAG600		M_DAG601		M_DAG602		M_DAG603		M_DAG604		M_DAG605		M_DAG606		M_DAG607		M_DAG608		M_DAG609		M_DAG610		M_DAG611		M_DAG612		M_DAG613		M_DAG614		M_DAG615		M_DAG616		M_DAG617		M_DAG618		M_DAG619		M_DAG620		M_DAG621		M_DAG622		M_DAG623		M_DAG624		M_DAG625		M_DAG626		M_DAG627		M_DAG628		M_DAG629		M_DAG630		M_DAG631		M_DAG632		M_DAG633		M_DAG634		M_DAG635		M_DAG636		M_DAG637		M_DAG638		M_DAG639		M_DAG640		M_DAG641		M_DAG642		M_DAG643		M_DAG644		M_DAG645		M_DAG646		M_DAG647		M_DAG648		M_DAG649		M_DAG650		M_DAG651		M_DAG652		M_DAG653		M_DAG654		M_DAG655		M_DAG656		M_DAG657		M_DAG658		M_DAG659		M_DAG660		M_DAG661		M_DAG662		M_DAG663		M_DAG664		M_DAG665		M_DAG666		M_DAG667		M_DAG668		M_DAG669		M_DAG670		M_DAG671		M_DAG672		M_DAG673		M_DAG674		M_DAG675		M_DAG676		M_DAG677		M_DAG678		M_DAG679		M_DAG680		M_DAG681		M_DAG682		M_DAG683		M_DAG684		M_DAG685		M_DAG686		M_DAG687		M_DAG688		M_DAG689		M_DAG690		M_DAG691		M_DAG692		M_DAG693		M_DAG694		M_DAG695		M_DAG696		M_DAG697		M_DAG698		M_DAG699		M_DAG700		M_DAG701		M_DAG702		M_DAG703		M_DAG704		M_DAG705		M_DAG706		M_DAG707		M_DAG708		M_DAG709		M_DAG710		M_DAG711		M_DAG712		M_DAG713		M_DAG714		M_DAG715		M_DAG716		M_DAG717		M_DAG718		M_DAG719		M_DAG720		M_DAG721		M_DAG722		M_DAG723		M_DAG724		M_DAG725		M_DAG726		M_DAG727		M_DAG728		M_DAG729		M_DAG730		M_DAG731		M_DAG732		M_DAG733		M_DAG734		M_DAG735		M_DAG736		M_DAG737		M_DAG738		M_DAG739		M_DAG740		M_DAG741		M_DAG742		M_DAG743		M_DAG744		M_DAG745		M_DAG746		M_DAG747		M_DAG748		M_DAG749		M_DAG750		M_DAG751		M_DAG752		M_DAG753		M_DAG754		M_DAG755		M_DAG756		M_DAG757		M_DAG758		M_DAG759		M_DAG760		M_DAG761		M_DAG762		M_DAG763		M_DAG764		M_DAG765		M_DAG766		M_DAG767		M_DAG768		M_DAG769		M_DAG770		M_DAG771		M_DAG772		M_DAG773		M_DAG774		M_DAG775		M_DAG776		M_DAG777		M_DAG778		M_DAG779		M_DAG780		M_DAG781		M_DAG782		M_DAG783		M_DAG784		M_DAG785		M_DAG786		M_DAG787		M_DAG788		M_DAG789		M_DAG790		M_DAG791		M_DAG792		M_DAG793		M_DAG794		M_DAG795		M_DAG796		M_DAG797		M_DAG798		M_DAG799		M_DAG800		M_DAG801		M_DAG802		M_DAG803		M_DAG804		M_DAG805		M_DAG806		M_DAG807		M_DAG808		M_DAG809		M_DAG810		M_DAG811		M_DAG812		M_DAG813		M_DAG814		M_DAG815		M_DAG816		M_DAG817		M_DAG818		M_DAG819		M_DAG820		M_DAG821		M_DAG822		M_DAG823		M_DAG824		M_DAG825		M_DAG826		M_DAG827		M_DAG828		M_DAG829		M_DAG830		M_DAG831		M_DAG832		M_DAG833		M_DAG834		M_DAG835		M_DAG836		M_DAG837		M_DAG838		M_DAG839		M_DAG840		M_DAG841		M_DAG842		M_DAG843		M_DAG844		M_DAG845		M_DAG846		M_DAG847		M_DAG848		M_DAG849		M_DAG850		M_DAG851		M_DAG852		M_DAG853		M_DAG854		M_DAG855		M_DAG856		M_DAG857		M_DAG858		M_DAG859		M_DAG860		M_DAG861		M_DAG862		M_DAG863		M_DAG864		M_DAG865		M_DAG866		M_DAG867		M_DAG868		M_DAG869		M_DAG870		M_DAG871		M_DAG872		M_DAG873		M_DAG874		M_DAG875		M_DAG876		M_DAG877		M_DAG878		M_DAG879		M_DAG880		M_DAG881		M_DAG882		M_DAG883		M_DAG884		M_DAG885		M_DAG886		M_DAG88	
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clamshell configuration



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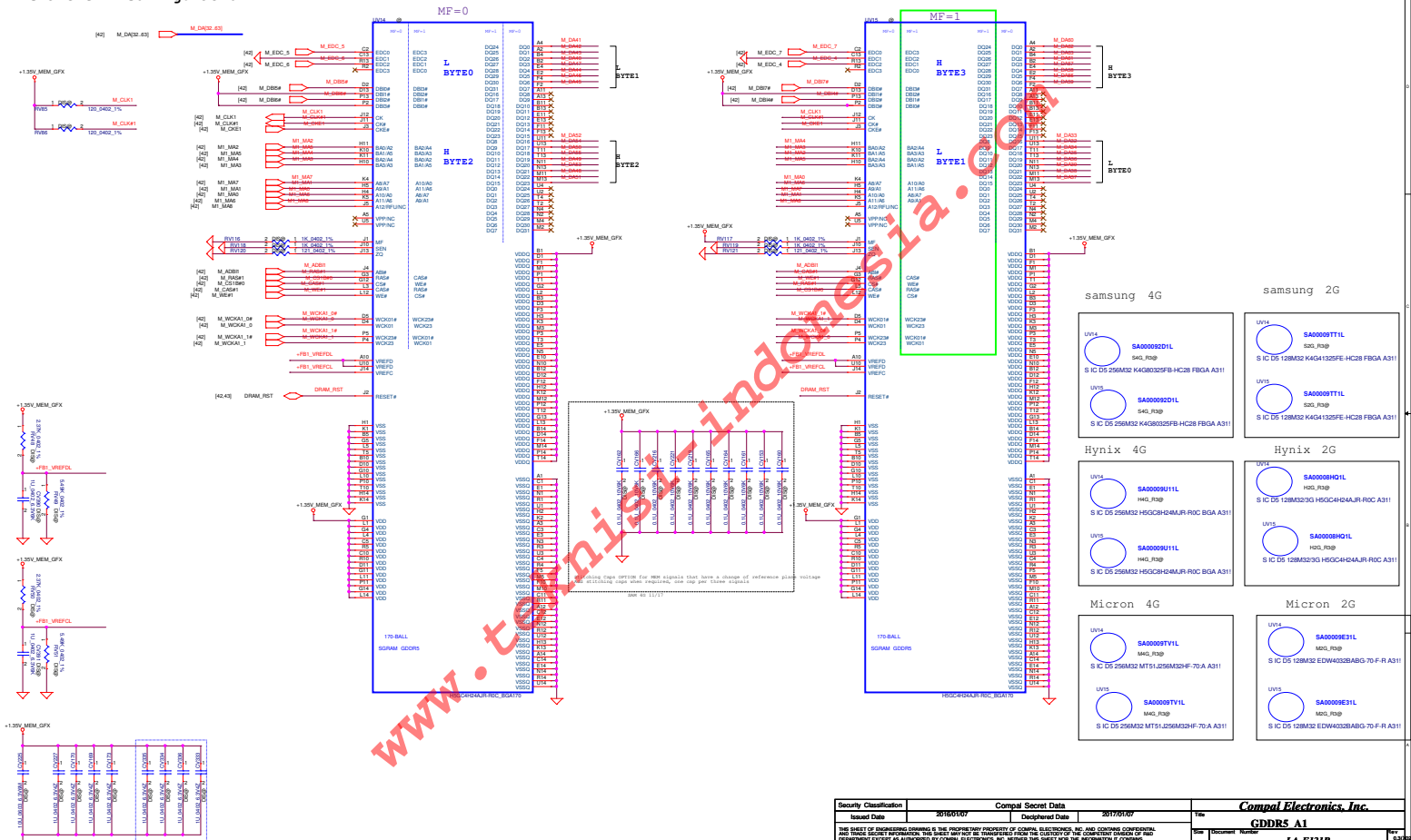
samsung 4G		samsung 2G	
U1V3	SA00009201L M4L_R0P S IC DS 256M32 K4G80325FB HC28 FBGA A311	U1V3	SA000097T1L S2L_R0P S IC DS 128M32 K4G41325FE HC28 FBGA A311
U1V3	SA00009201L M4L_R0P S IC DS 256M32 K4G80325FB HC28 FBGA A311	U1V3	SA000097T1L S2L_R0P S IC DS 128M32 K4G41325FE HC28 FBGA A311
Hynix 4G		Hynix 2G	
U1V3	SA000090U1L M4L_R0P S IC DS 256M32 H5G0C4H4AJR ROC BGA A311	U1V3	SA00008HQ1L H5L_R0P S IC DS 128M32G H5G0C4H4AJR ROC A311
U1V3	SA000090U1L M4L_R0P S IC DS 256M32 H5G0C4H4AJR ROC BGA A311	U1V3	SA00008HQ1L H5L_R0P S IC DS 128M32G H5G0C4H4AJR ROC A311
Micron 4G		Micron 2G	
U1V3	SA00009TV1L M4L_R0P S IC DS 256M32 MT11J256M32HF-70-A A311	U1V3	SA00008E31L M4L_R0P S IC DS 128M32 EDW4032BAG-70-F-R A311
U1V3	SA00009TV1L M4L_R0P S IC DS 256M32 MT11J256M32HF-70-A A311	U1V3	SA00008E31L M4L_R0P S IC DS 128M32 EDW4032BAG-70-F-R A311

Security Classification	Compal Secret Data	Issued Date	Discontinued Date	2017/01/07
2016/01/07				

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Issued Date		Deciphered Date		Title GD8RS A1	
2016/10/07		2017/01/07		Date Dec 12, 2017	
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Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as 750 mV/ μ s).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.

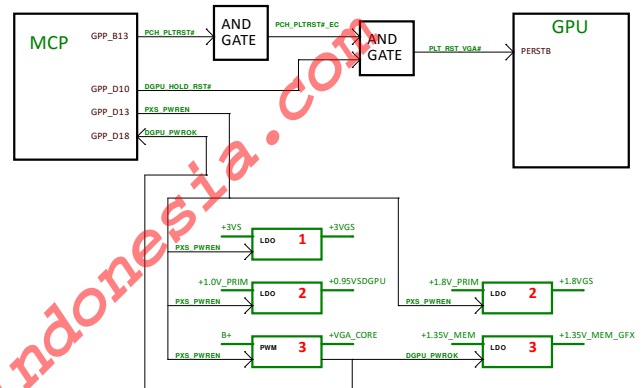
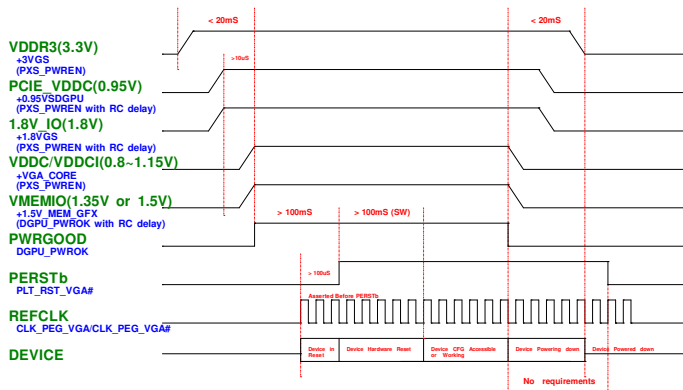


Table 3-21 Resistor Divider Lookup T

R _{pu} (Ω)	R _{pd} (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

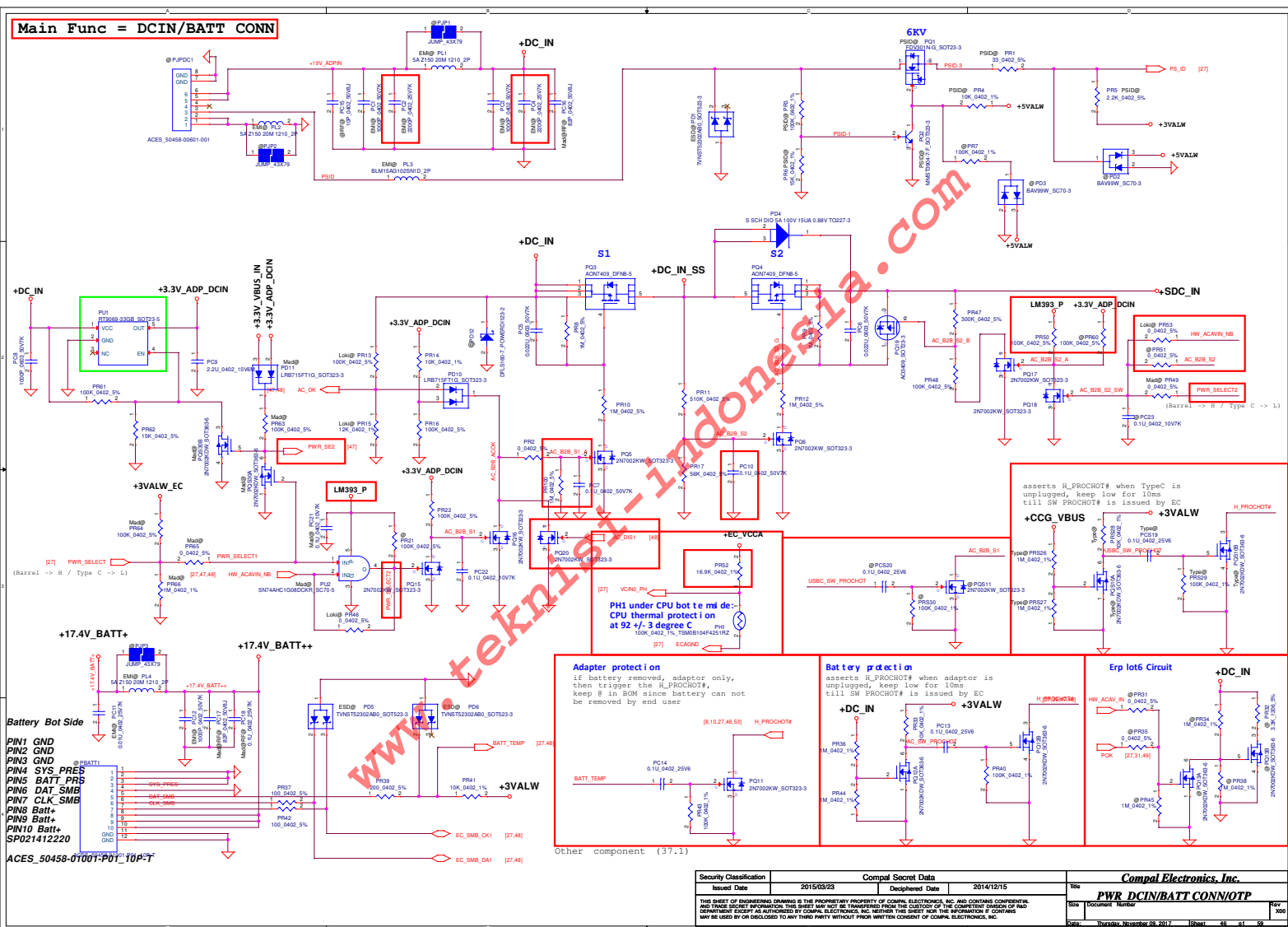
Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only

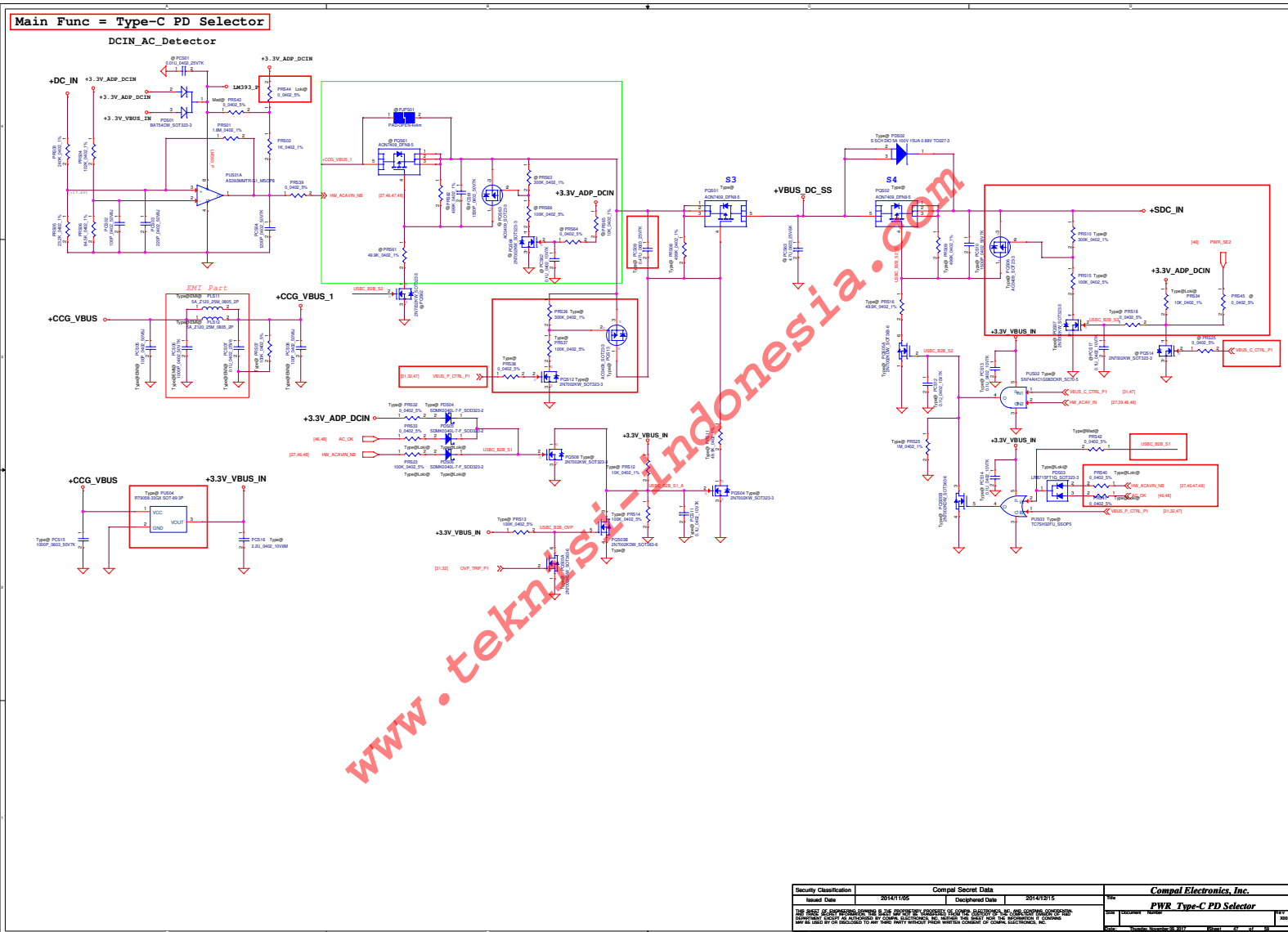
Memory ID	R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24JR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BAG-70-F-R A31!	2GB

Memory ID	R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70-A A31!	4GB

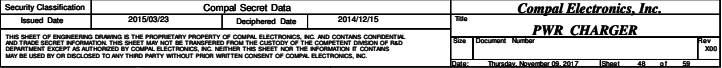
Security Classification	Compal Secret Data	Deciphered Date	Deciphered Date	Rev
Issued Date	2016/01/07	Deciphered Date	2017/01/07	0.3
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<p>Compal Electronics, Inc.</p> <p>M30/M70 NOTE</p> <p>LA-F121P</p>				0.3



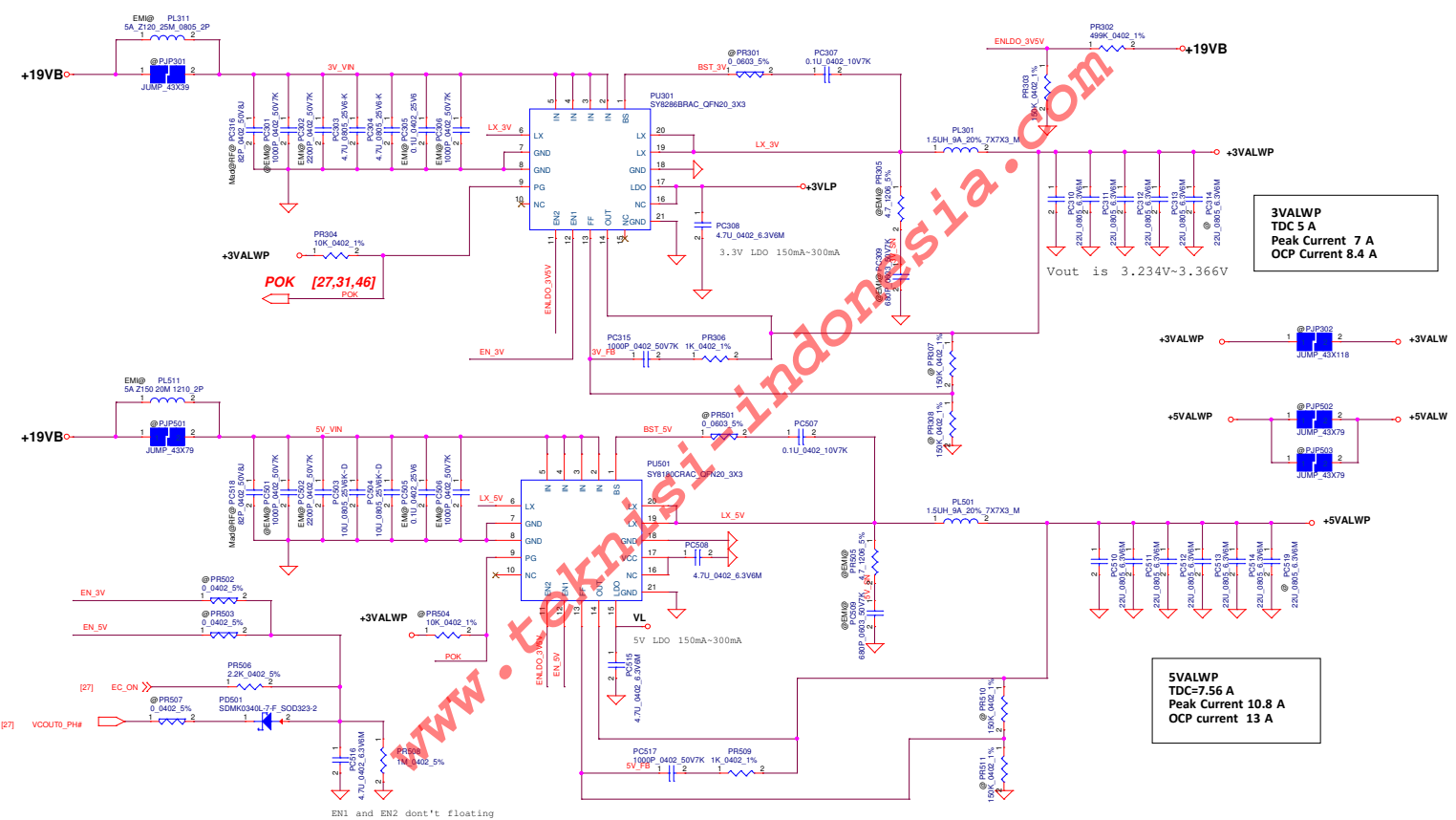
Security Classification	Control Secret Data		Title	
Issued Date	2015/02/23	Declassified Date	2014/12/15	
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Size	11x17	Sheet	48	of 59




Main Func = CHARGER

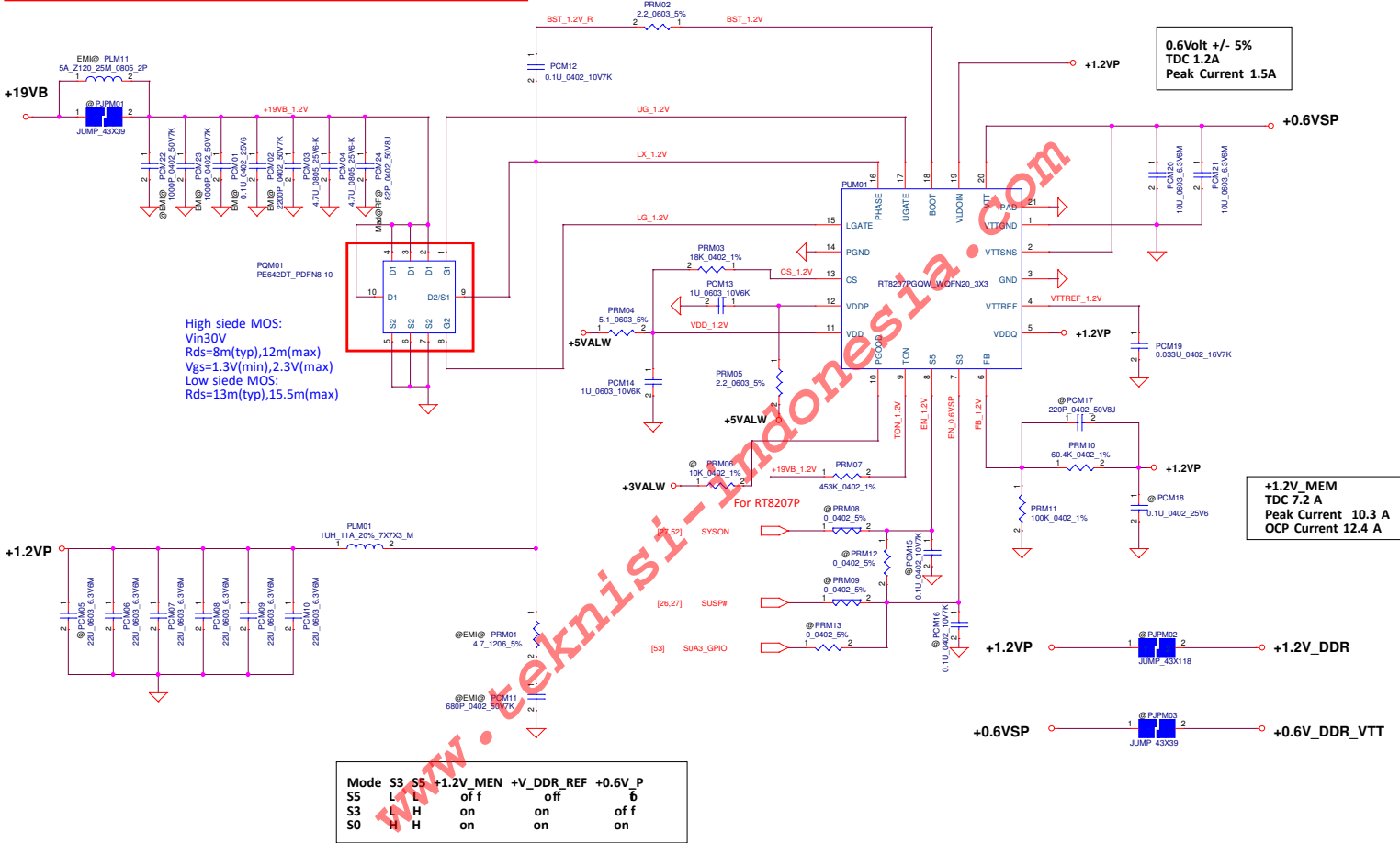


Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data			
Issued Date	2014/2/11	Deciphered Date	2014/2/11	Title
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Date:	Thursday, November 06, 2017		Sheet	49 of 59

Main Func = +1.2V_DDR/+0.6V_DDR_VTT

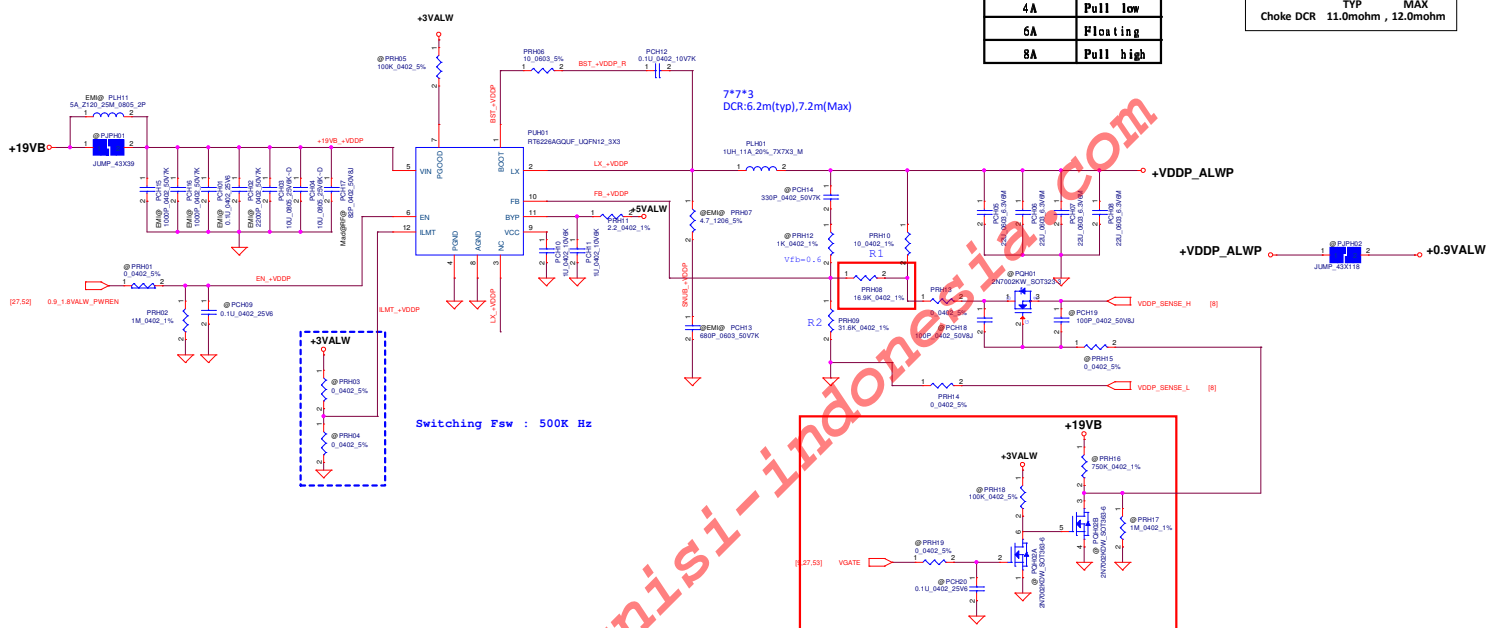


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title
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Date: Thursday, November 08, 2017				Sheet 50 of 59

The current limit is set to 4A, 6A or 8A when this pin is pull low, floating or pull high

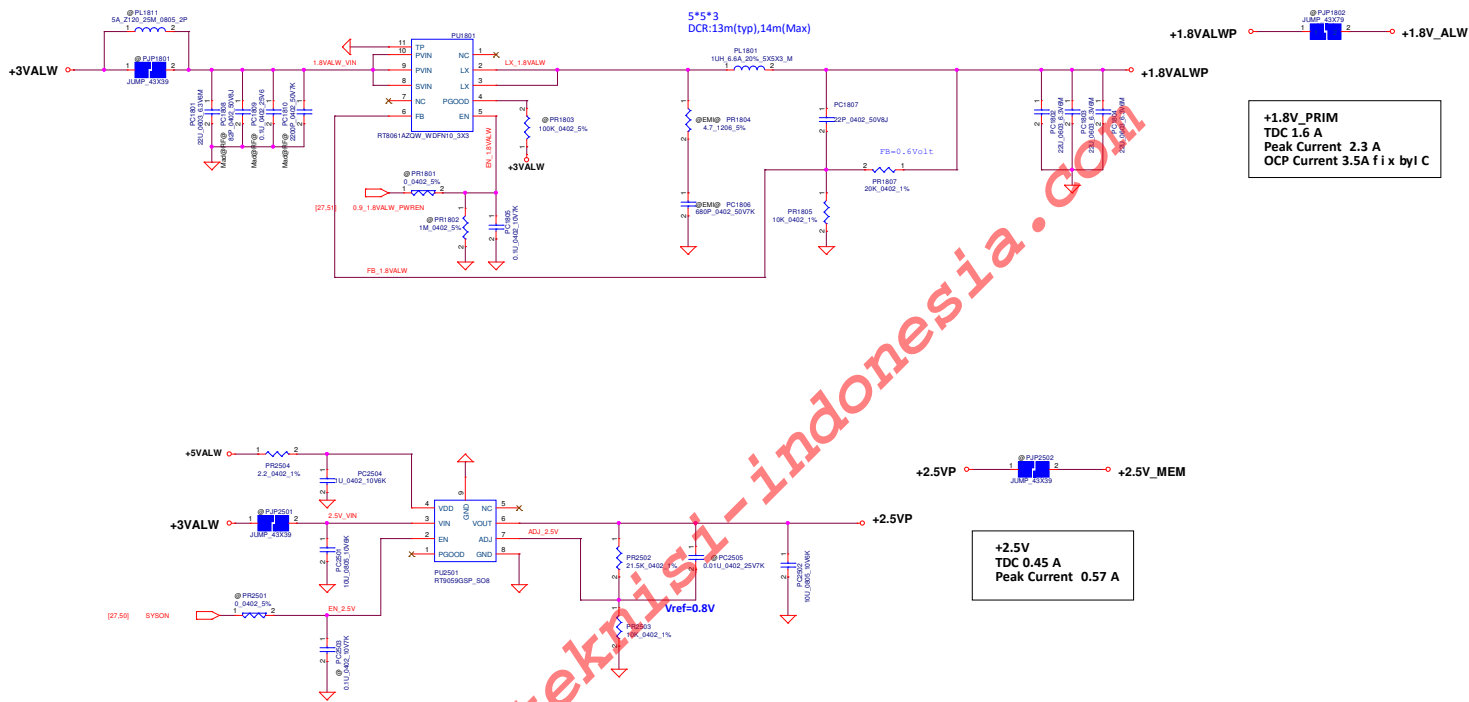
OCP setting	ILMT(pin3)
4A	Pull low
6A	Floating
8A	Pull high

+VDDP_ALWP
TDC 4 A
Peak Current 5 A
OCP Current 6 A Fix by IC
Choke DCR 11.0mohm, 12.0mohm



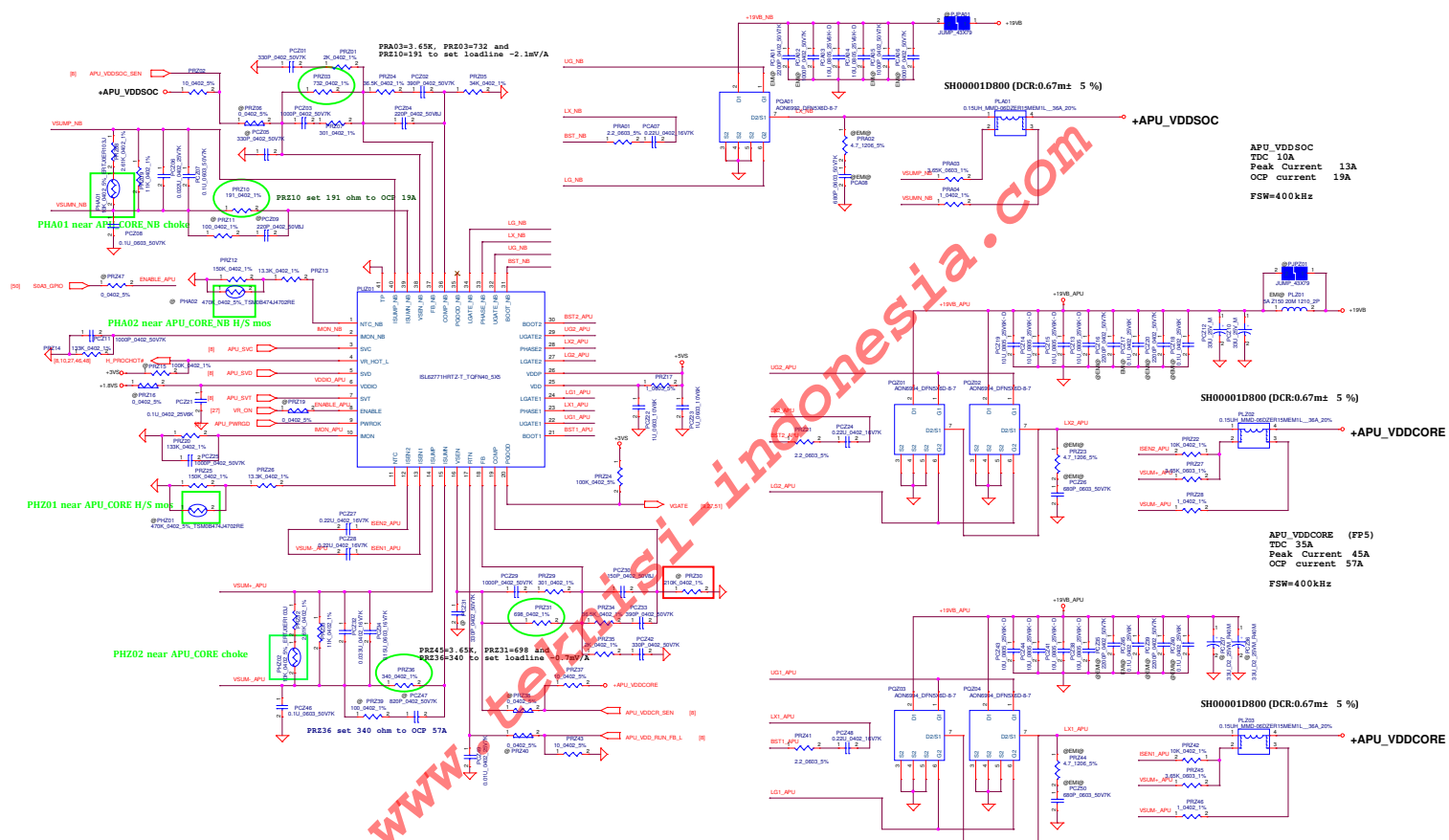
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title	PWR +VDDP ALWP
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Date				D	3000
Thursday, November 08, 2017 19:00 51 of 58					

Main Func = +1.8VALWP / +2.5VP



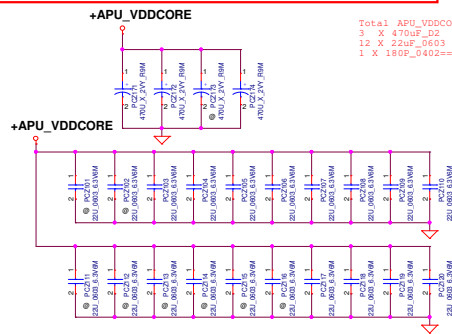
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	
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Rev	Document Number	Title		Rev
C		PWR +1.8V PRIM and +2.5V		300
Notes	November 05, 2017		Sheet	53 of 58

Main Func = APU_VDDCORE / APU_VDDSOC

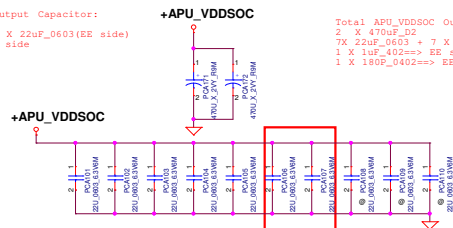


Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2013/01/04		Depaginated Date		2015/01/04		Title	
								PWR APU CORE/APU CORE NB	
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Date	Drawing Number			Sheet			of		
Rev	Drawing Number			Sheet			of		

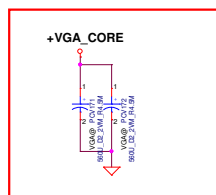
Main Func = APU/ VGA / APU_SOC MLCC



```
Total APU_VDDCORE Output Capacitor:
3 X 470uF_D2
12 X 22uF_0603 + 16 X 22uF_0603(EE side)
1 X 180P_0402==> EE side
```



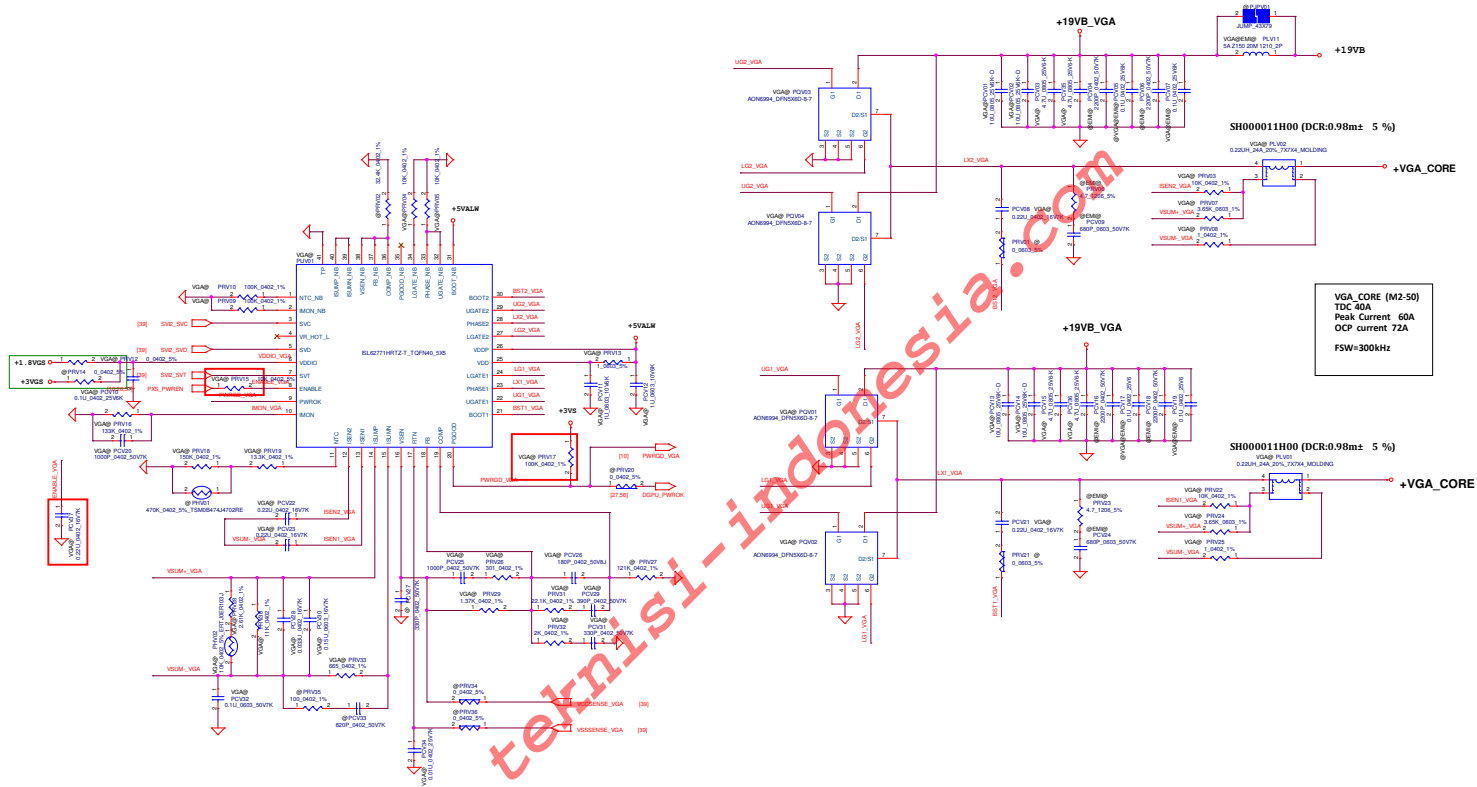
```
Total APU_VDDSOC Output Capacitor:
2 X 470uF_D2
7X 22uF_0603 + 7 X 22uF_0603(EE side)
1 X 1uF_402==> EE side
1 X 180P_0402==> EE side
```



For VGACORE

Security Classification	Compal Secret Data		<i>Compal Electronics, Inc.</i>	
Issued Date	2014/11/05	Deciphered Date	2014/12/15	The
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Date:	Document Number	Sheet	of	Rev
2014/11/05	001	01	01	X00

Main Func = VGA CORE



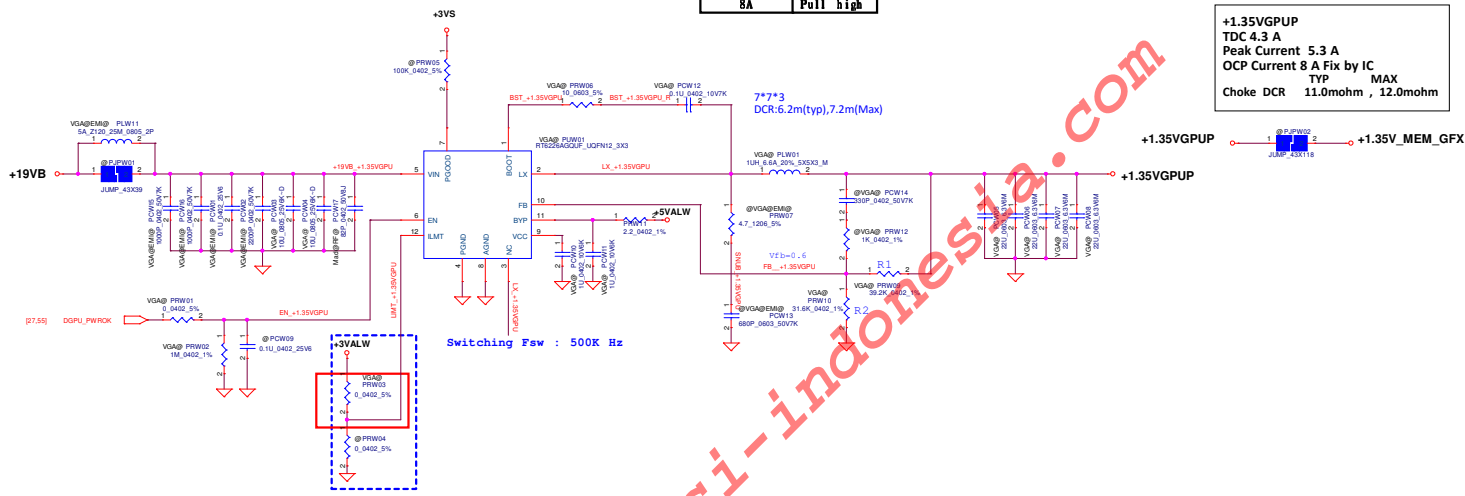
VGA_CORE (M2-50)
TDC 40A
Peak Current 60A
OCP current 72A
FSW=300kHz

Security Classification		Control Secret Data		Compal Electronics, Inc.	
Issued Date	2014/1/05	Discontinued Date	2014/9/15	Title	
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				Rev	Rev
				Date	Thursday, November 28, 2012 10:11 AM

Main Func = +1.35VGPUP

OCP setting	ILMT(pin3)
4A	Pull low
6A	Floating
8A	Pull high

+1.35VGPUP	
TDC 4.3 A	
Peak Current 5.3 A	
OCP Current 8 A Fix by IC	
	TYP MAX
Choke DCR	11.0mohm , 12.0mohm



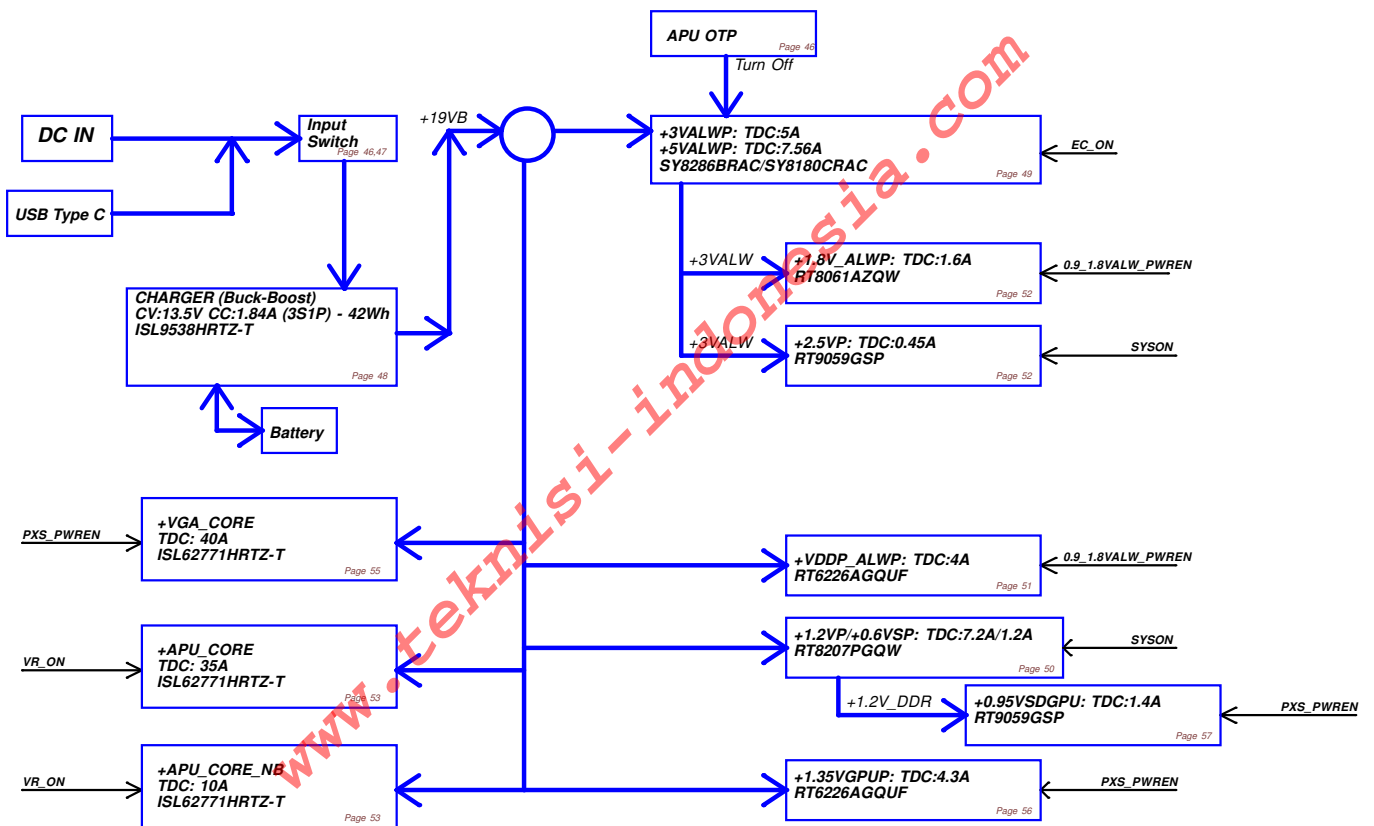
www.teknisi-indonesia.com

Security Classification	Compal Secret Data	Deciphered Date	2015/04/30	Compal Electronics, Inc.	
Issued Date	2014/03/31	Deciphered Date	2015/04/30	Title	
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Rev	Document Number			Rev	
001	001			001	
001	001			001	

[illegible]

Security Classification	Compal Secret Data			Title
Issued Date	2015/03/23	Deciphered Date	2014/12/15	PWR +0.95VSDGPU
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Doc Number				Revision Number
Date	Issued / Deciphered / Rev 007 / 0000			47 / n / 58

Power block



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	
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				Date	Thursday, November 09, 2017
				Sheet	58 of 58

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P46	PWR	20170704	COMPAL	EMI test result for change capacity	change PC2,PC4 from 0.1u to 2200p	0.2 (X01)
2	P55	PWR	20170704	COMPAL	Request by EE for adjust DGPU sequence	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2 (X01)
3	P48	PWR	20170704	COMPAL	support FTRD 1.6 and LPS from EC request	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2 (X01)
4	P47	PWR	20170704	COMPAL	add fast close MOS	pop PQS06, PQS07, PQS13, PRS10, PRS15, PRS18, PRS36, PRS37, PRS38, PRS40, PRS41	0.2 (X01)
5	P46	PWR	20170710	COMPAL	for LPS SW solution	add PQ20	0.2 (X01)
6	P51	PWR	20170717	COMPAL	adjust output to 0.9V by EE request	change PRH08 from 10.7K to 15.8K	0.2 (X01)
7	P46	PWR	20170917	COMPAL	follow Intel design	pop PR53 and unpop PR51	0.3 (X02)
8	P46	PWR	20170917	COMPAL	follow Intel design	unpop PC23, PQS11, PRS30, PCS20 add PR100 1M	0.3 (X02)
9	P54	PWR	20170918	COMPAL	for PSI_Dynamic test with AMD validation	pop PCA106, PCA107	0.3 (X02)
10	P48	PWR	20170918	COMPAL	follow Intel design	unpop PCB46	0.3 (X02)
11	P51	PWR	20170918	COMPAL	for VDDP_Static test with AMD validation	change PRH08 from 15.8K to 16.9K	0.3 (X02)
12	P46	PWR	20170920	COMPAL	follow Intel design	change PC7, PC10 from 0.1U_10V to 0.1U_50V	0.3 (X02)
13							

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/22	Deciphered Date	2017/01/31	Title	Changed-List PWR History
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				Date:	Thursday, November 09, 2017
				Sheet	69 of 69

Security Classification		Compul Secret Data		<i>Compul Electronics, Inc.</i> <i>Charged-List PWR History</i>	
Issued Date	2015/12/22	Deciphered Date	2017/01/31	Title	
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				Date:	Thursday, November 09, 2017
				Sheet	81 of 89
				Rev	X00

DVT1 change list

BOM change list

BOM Change								
Item	Date	Page	Part reference	Original CPN	New CPN	Change description	Reason	
1	2017/6/2	33	RT52,RT53			bom structure from typec@ change to @	fix the typec i2c signal about DP out	
2	2017/6/3	27	RE6			bom structure from notypec@ change to pop always	fix dead battery auto wakeup	
3	2017/6/3	27	RE508			bom structure from typec@ change to @	fix dead battery auto wakeup	
4	2017/6/19	27	RE9	SD034000080	SD034150280	0 ohm change to 15K	EC board id(UMA)	
5	2017/6/19	27	RE9	SD034120280	SD034200280	12k change to 20K	EC board id(DSC)	
6	2017/6/20	9	RC29,CC7,RC700			change to pop(PCIE_RESET_0)	fixed pcie rst singal	
7	2017/6/20	9	RC704,CC100,RC701			change to unpop(PCIE_RESET_1)	pcie rst_1 signal code not ready	
8	2017/7/6	10	C796	SE07156AD80	SE07147AC80	change part from 5.6P to 4.7P	fixed crystal accuracy	
9	2017/7/6	10	C797	SE07156AD80	SE000011R00	change part from 5.6P to 3.9P	fixed crystal accuracy	
10	2017/7/6	9	D5,D6		SCS00000Z00	add part (diode)	fix Panel will flash white screen when press power button (Bits333224)	
11	2017/7/12	29	Q26		SB00000DH00	add part (dual mos) reserve	follow loki intel led design	
12	2017/7/12	29	R82,R83		SD028100380	add part(100K) reserve	follow loki intel led design	
13	2017/7/12	29,34	R800,R862		SD028000080	add part(0 ohm)	follow loki intel led design	
14	2017/7/12	23	CU38,CU39,CU40,CU41		SE00000P700	add part 0.33U	follow AMD require to add 0.33U Cap	
15	2017/7/12	23	CU7,CU8,CU15,CU16	SE102104K00	SE095224K00	change part(0.1U to 0.22U)	follow AMD require to change to 0.22U Cap	
16	2017/7/13	10	RC449	SD028330A80	SD028220A80	change part 33 ohm to 22 ohm	follow AMD SCL F04	

GPIO change list

Signal for PCH				
Date	GPIO	Pin Definition		Reason
		R0.1(X00)	R0.2(X01)	
2017/6/3	AGPIO11	NC	MEM_ERROR_A	Memory error detection(Bits334733)
2017/7/4	AGPIO12	NC	MEM_ERROR_B	Memory error detection(Bits334733)
2017/7/4	EGPIO 70	NC	VBIOS_ID1	old GPIO SW no support
2017/7/10	AGPIO89	PXS_RST#	NC	fixed GPU Yellow bang
2017/7/10	AGPIO90	PXS_PWREN	KB_DET#	fixed GPU Yellow bang
2017/7/10	AGPIO86	PWRGD_VGA	NC	fixed GPU Yellow bang
2017/7/10	EGPIO 140	KB_DET#	PXS_RST#	fixed GPU Yellow bang
2017/7/10	EGPIO 141	NC	PXS_PWREN	fixed GPU Yellow bang
2017/7/10	EGPIO 143	NC	PWRGD_VGA	fixed GPU Yellow bang

KBC ENE 9022				
Date	GPIO	Pin Definition		Reason
		R0.1(X00)	R0.2(X01)	
2017/6/3	AGPIO0	NC	MEM_ERROR_A	Memory error detection(Bits334733)
2017/7/4	AGPIO39	NC	MEM_ERROR_B	Memory error detection(Bits334733)

Design change list

Design Change					
Item	Date	Page	Part reference	change description	Reason
Based on EVT					
1	2017/6/2	29		BATT_CHG_LED from R68.2 to R69.2 ,BATT_LOW_LED from R69.2 to R68.2	correct led color indication
2	2017/6/19	32		DT3~DT10 change footprint	meet DFB
3	2017/6/29	33		JUSBC1 change footprint	meet DFB
	2017/7/6	9		add D5,D6	fix Panel will flash white screen when press power button (Bits333224)
4	2017/7/11	36		JCRT from 20P coaxil to 16P ZIF	follow loki intel
5	2017/7/12	23		add RX cap footprint for usb compatible	follow AMD require
6	2017/7/12	29,34		add nvme led status circuit(reserve)	follow loki intel

DVT2 change list

BOM change list

BOM Change								
Item		Date	Page	Part reference	Original CPN	New CPN	Change description	Reason
1		2017/9/4	32	D2	SCA00001G00		unpop	follow ESD require
4		2017/9/4	27	RE9	SD034150280	SD034270280	15K change to 27K	EC board ID
5		2017/9/4	27	RE9	SD034200280	SD034330280	20K change to 33K	EC board ID
12		2017/9/4	11	RC801	SD028100580		add 10M	follow factory require for RTC detect
13		2017/9/4	11	QC27	SB00000EN00		add mos	follow factory require for RTC detect
14		2017/9/4	9	RC6130	SD028100280		add 10K	follow factory require for RTC detect
15		2017/9/8	18	CA50,CA51	SE071100J80		change to pop	follow EMI require
16		2017/9/18	33	RT132,RT133	SD028000080		add 0 ohm	follow SCL1.05

GPIO change list

Signal for PCH								
Date	GPIO	Pin Definition		Reason				
		R0.2(X01)	R0.3(X02)					
	AGPIO7	NC	RTC_DET#	factory require				
	AGPIO76	SPI_IRQ#	NC	PSP related GPIO				
	AGPIO30	NC	SPI_IRQ#	PSP related GPIO				
	EGPIO121	BT_ON#	NC	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.				
	EGPIO120	NC	BT_ON#	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.				

Design change list

Design Change							
Item	Date	Page	Part reference	change description	Reason		
Based on DVT1							
1	2017/9/4	11	QC27,RC801,RC6130	add RTC coin battery detect circuit	for factory require		
2	2017/9/4	27	RE9	UMA form 15K to 27K, DIS from 20K to 33K	EC board ID		
3	2017/9/4	10,20	RC902	reserve (0 ohm)	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.		
4	2017/9/12			I2C0 change to I2C3	BITS332966 ULV-Loki-AMD: Lost some items in Touchpad setting.		
5	2017/9/18	33	RT132,RT133	add series resistor for APU_DP3_AUXP/APU_DP3_AUXN	follow SCL 1.05		